Designing Multi-Cell Li-ion Battery Packs Using the ISL9216, ISL9217 Analog Front End

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Description

This application note discusses some of the hardware and software design decisions and shows how to select external components for a multi-cell, Li-ion battery pack using a microcontroller and the ISL9216 and ISL9217 analog front end chip set.

A microcontroller provides the primary control of the operation of the battery pack. However, several factors in the multi-cell series Li-ion pack require the use of circuitry around the microcontroller. They are:

- The voltages involved in a multi-cell series battery pack (more than 50V for twelve cells in series), are far higher than most microcontrollers are rated. So, the pack needs a voltage regulator to power the microcontroller. The microcontroller cannot just operate on the voltage from one of the string of Li-ion cells (typically 3.0V to 4.2V) because higher current from only one cell will cause an imbalance in the battery pack. This will shorten the life of the pack. A later discussion highlights the effects of unbalanced cells and how to rebalance the pack.
- The high voltage of the cells in the pack precludes the microcontroller from reading the voltage on each cell as needed to properly manage the charge and discharge limits in each cell. So the pack needs circuits that level shift the voltages across each cell down to a ground referenced voltage that the microcontroller can read using its internal analog to digital (A/D) converter.
- Because the microcontroller is relatively slow to respond to high speed overcurrent events (such as a short circuit condition), the pack needs circuits that shut down the pack quickly and autonomously of the microcontroller in order to protect the cells and the electronics in the pack.
- In order to balance the cells in the pack, the microcontroller needs circuitry that will activate the balancing circuit of each cell. Most of these circuits are at a voltage too high for direct microcontroller control.

The ISL9216 and ISL9217 chip set meets all of these needs and supports battery pack configurations consisting of 8-cells to 12-cells in series and one or more cells in parallel.

The ISL9216, ISL9217 is a very flexible chip set that can be used in a variety of ways to implement the battery pack. The ISL9216 provides integral overcurrent protection circuitry, short circuit protection and drive circuitry for external FET devices that control pack charge and discharge. Both the ISL9216 and the ISL9217 provide an internal 3.3V voltage regulator, internal cell balancing switches, cell voltage monitor level shifters, and status indicators. Each of these features have some flexibility in how they are used.

Battery Connection

The ISL9216, ISL9217 supports multiple series connected Li-ion cells. The bottom three cells of each device (CELL1, CELL2, and CELL3) must be connected to a battery cell. The top cell in the string must also be connected to the ISL9217. The ISL9216 VCC pin needs to connect two cell voltages above the ISL9217 VSS. Connections to CELL4 and CELL5 of both devices and CELL6 of the ISL9217 are optional. This allows the ISL9216, ISL9217 to be used in battery packs of 8-cells to 12-cells[1]. Connection guidelines for each cell combination are shown in Figure 2.

If possible, when connecting the cells to the pack, provide separate “Kelvin” connections from the cell to the VCELLN pin. This is to minimize the change in input voltage when the cell balance circuit turns on. For example, see Figure 1. This connection will reduce by half the input variation of a cell that is also being balanced. The difference between the cell voltage when being balanced and when not being balanced may still be significant enough that cell measurement can only be made when not balancing.

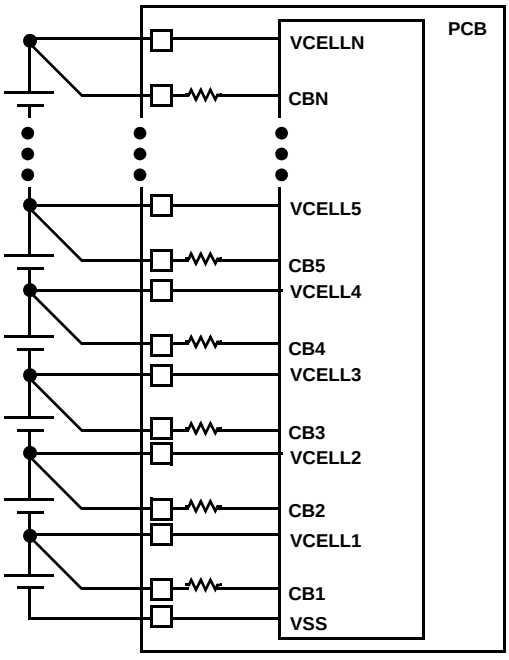
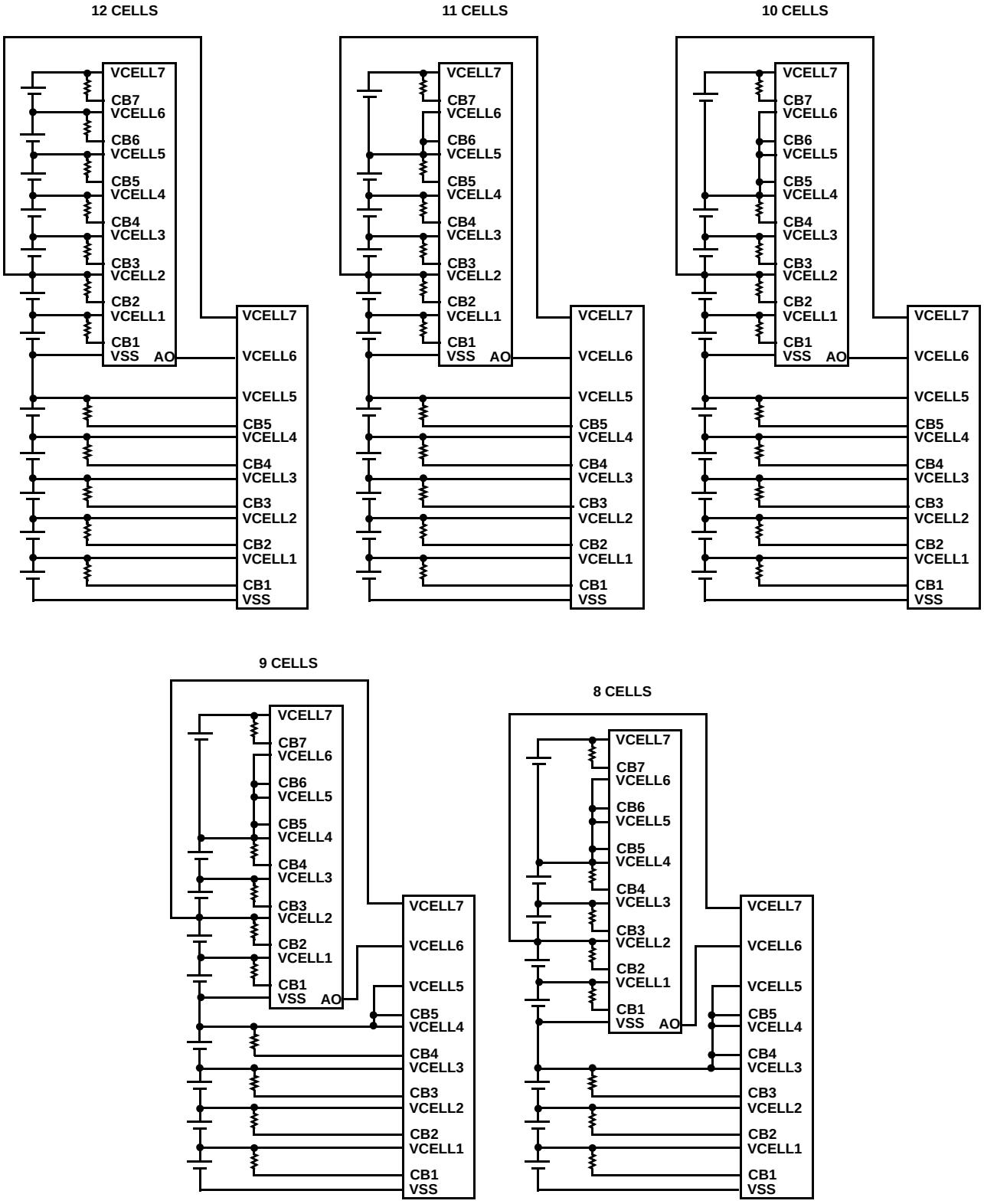


FIGURE 1. CELL AND CELL BALANCE WIRING WITH VCELL KELVIN CONNECTION

1. The ISL9216, ISL9217 could support battery packs with fewer than 8-cells per pack, but these would be better served by the ISL9208 device.



Note: Multiple cells can be connected in parallel

FIGURE 2. BATTERY CONNECTION OPTIONS

System Power Up/Power Down

The cells can also be connected in other sequences as long as the VCELL inputs are eventually connected with:

$$VCELL12 \geq VCELL11 \quad VCELL11 \geq VCELL10$$
$$VCELL10 \geq VCELL9 \quad VCELL9 \geq VCELL8$$
$$VCELL8 \geq VCELL7 \quad VCELL7 \geq VCELL6$$
$$VCELL6 \geq VCELL5 \quad VCELL5 \geq VCELL4$$
$$VCELL4 \geq VCELL3 \quad VCELL3 \geq VCELL2$$
$$VCELL2 \geq VCELL1 \quad VCELL2 \geq VSS$$

(EQ. 1)

Each cell input voltage differential never exceeds the specified limit, as shown in the data sheet FN6488.

When connecting the cells from bottom to top, once cells 1, 2, and 3 are connected to the board, the ISL9216 regulator may try to turn on[2]. Depending on the current needed by the external circuits, and without a VCC connection, the regulator may not be able to maintain regulation and could turn off. There is a possibility that this starts a turn on/turn off oscillation in the power supply until all of the cells in the pack are connected.

If the regulator does power-up with only the VCELL1, VCELL2, and VCELL3 pins connected, then the microcontroller software starts up. If the microcontroller has code that puts the pack to sleep when a cell voltage is too low, then the pack could go to sleep immediately on initial connection of these three cells.

One way to avoid these initial power-down conditions is to connect the ISL9216 cells from the top down (VCC to VSS). In this way, the voltage regulator does not power-up until all cells are connected. Another way to handle this is in software, with the code waiting a while before shutting down in response to a low cell voltage.

The ISL9216 and ISL9217 devices each power up when the voltages on VCELL1, VCELL2, VCELL3, and VCC all exceed their POR threshold. At that time, the devices attempt to turn on their respective RGO outputs. Before the ISL9216 RGO output turns on, however, all cells may need to be connected to provide the external regulator voltage.

The ISL9216 RGO provides a regulated 3.3VDC voltage at the RGO pin. It does this by using a control signal on the RGC pin to drive an external NPN transistor. The transistor should have a beta of at least 70 to provide ample current to the device and external circuits and should have a V_{CE} of greater than 60V (preferably 80V) for a 12-cell pack.

2. The data sheet indicates that VCC needs to be at least 9.2V to guarantee power-up of the ISL9216. However, VCC may only need to be 4V before power on can happen. Because of the internal ESD structures on the CBn inputs and assuming there are cell balance resistors, as shown in Figure 2, connecting CELL1, CELL2, and CELL3 may apply enough voltage on VCC to reach the turn-on threshold.

The ISL9217 RGO also provides a regulated 3.3V, relative to the ISL9217 VSS pin. The ISL9217 also requires an external NPN transistor, however, this transistor does not need to supply much external current so its gain is not too important. In this case, the transistor should have a V_{CE} of greater than 40V (preferably 50V) for a 12-cell pack.

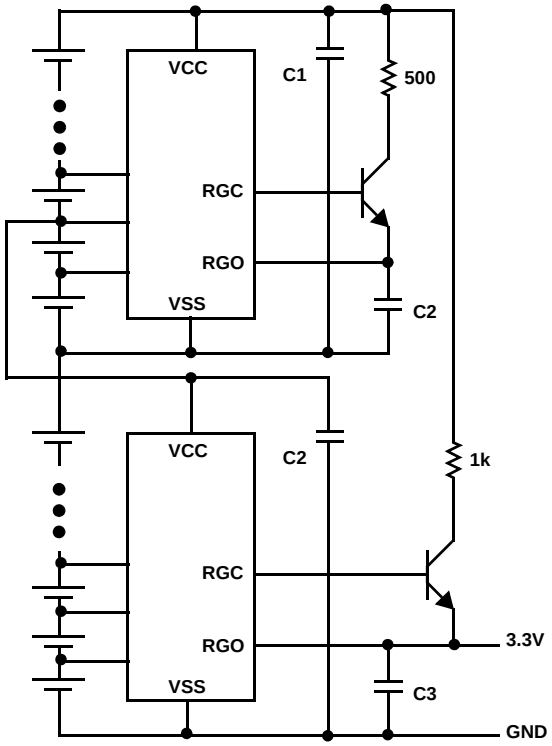


FIGURE 3. VOLTAGE REGULATOR CIRCUITS

A 500Ω resistor is recommended in the collector of the ISL9217 NPN transistor and a 1kΩ resistor is recommended in the collector of the ISL9216 NPN transistor to minimize initial current surge when the regulator turns on and provide current limiting in the event that the transistor fails.

Without the collector resistors, the initial turn-on current surge could be large. If there is also a relatively high resistance on the VCC input and if the VCC capacitor is too small, then the initial application of power can cause the voltage at VCC to drop momentarily. If this voltage drops below the minimum VCC power-up voltage, then the regulator may start to turn off. As it does, the current drops and the VCC voltage rises, again starting the regulator. This “oscillation” could prevent proper power-up of the ISL9216. In a normal battery pack operation, this oscillation is not likely, because the battery cell has a very low impedance.

The collector resistors also serve another function. They help to protect the Q_1 transistor from excessive voltage and current and minimize the consequences of a failure in Q_1.

There are some limitations in the cell connection order. The problem lies in the “random” cell connection. In this case, it is possible that the cell 6 or the cell 11 connection and VSS

are the first two connections. If this happens, the capacitor on VCC is charged at high voltage through the CB7 cell balance ESD structure and cell balancing resistor. If the capacitor is large enough and the series resistance small enough, the energy dissipation in the CB7 structure (as a result of the surge current) will cause a failure inside the ISL9216 or ISL9217. Higher cell balancing resistors prevent this, but this also limits the effectiveness of cell balancing. See Figure 4.

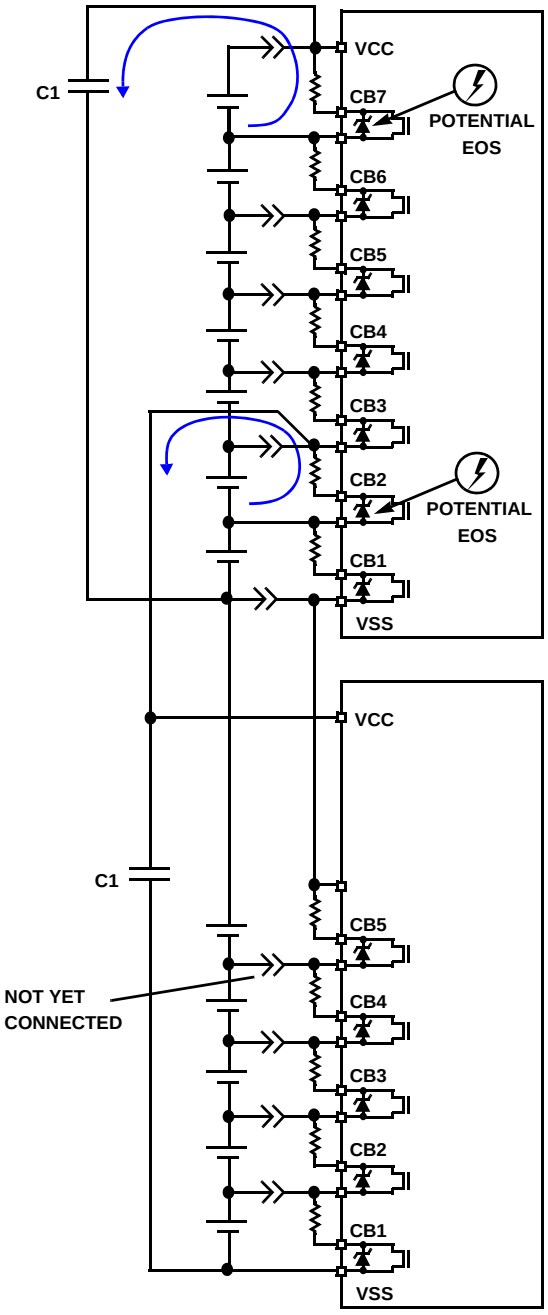


FIGURE 4. CONNECTION SEQUENCE CAUTION

Adding a series resistor on each of the cell inputs reduces the initial current surge through the ISL9216 or ISL9217 inputs. However, this needs to be carefully considered because adding series resistance effects the accuracy of the cell measurements. A series resistance of 15Ω will add about 1mV of error to the cell voltage reading. It is possible that this error can be calibrated out, but it also requires that external cell balancing FETs be added. For more information about this, see “Input Filtering” on page 24.

Another condition that can effect the proper operation of the ISL9216 and ISL9217 is when a motor being powered by the pack turns off. This has the potential for generating significant noise. This noise (if it reaches the VCELL1 input) can cause the loss of the internal register contents. Prevent this with the use of a 4.7µF capacitor (or larger) in parallel with a 0.01µF capacitor being connected between VCELL1 and GND.

For development work, or if the sequence of cell connections cannot be guaranteed, or if there are potential voltage excursions on the cell inputs that violate the specified 5V maximum, the use of 4.7V zener diodes across each cell input is recommended. These diodes protect the cell inputs from both the maximum cell voltage and the input surge current.

The best trade-off is to use:

- A 0.01µF capacitor on VCC
- A parallel combination of 4.7µF and 0.1µF caps on VCELL1
- A 500Ω series resistor on the ISL9217 NPN collector and 1kΩ series resistor on the ISL9216 NPN collector
- 4.7V zener diodes on each cell input (unless cells connect in sequence. See Figure 5).

In addition to the VCELL1 capacitors, the microcontroller code should periodically check the ISL9216 register contents and reload the desired values, if they have changed.

The ISL9217 also has internal registers that could be effected by noise, so capacitors are also recommended on the VCELL1 input. However, the ISL9217 registers do not contain any “pack critical” parameters, so the capacitors are less important.

Once powered up, the device remains in a wake up state until put to sleep by the microcontroller or until the VCELL1, VCELL2, VCELL3, or VCC voltages on each device drop below their POR thresholds.

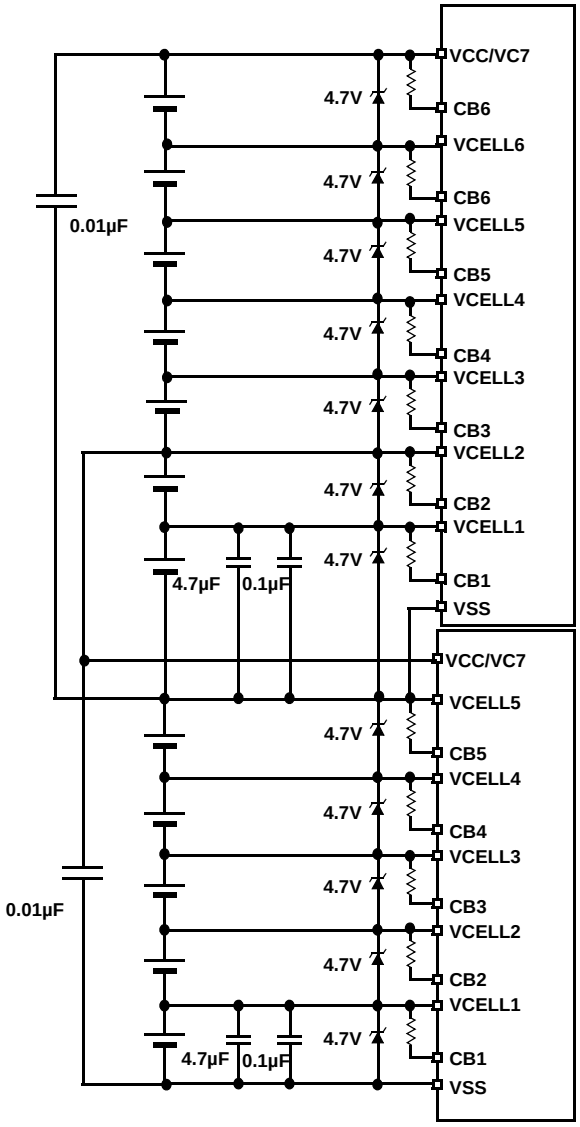


FIGURE 5. RECOMMENDED INPUT CONNECTIONS

Voltage Regulator

The ISL9216 can provide 350µA or more of output current to the RGC pin. Using an NPN transistor with a gain of 100, the ISL9216 regulator can supply up to 35mA to an external load and maintain the output at 3.3V, ±10%. A typical external load of 3mA and a transistor gain of 100 results in the ISL9216 supplying 30µA to the NPN transistor base.

The voltage at the emitter of the NPN transistor is monitored and regulated to 3.3V by the control signal at RGC. The RGO voltage also powers many of the ISL9216 internal circuits.

Following is some characterization data gathered over 30 units (data from ISL9216). This shows the regulation accuracy at no load and at a “maximum” load of 35mA (assuming an NPN transistor with a gain of 100). Typically, the load will be much less than the maximum load, so the variation of RGO will be much less. But, if the microcontroller A/D converter accuracy is dependent on the RGO voltage, then a calibration step is likely needed to trim the accuracy of the A/D for cell voltage measurements. Generally, this calibration can be done once at room temperature because the variation over-temperature is low. However, for measurements more accurate than ±25mV at a cell voltage of 4.2V, a voltage reference is recommended.

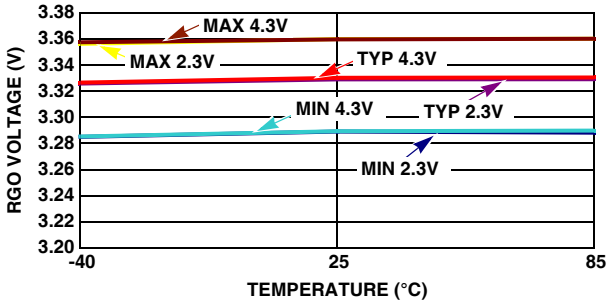


FIGURE 6. RGO REGULATION OVER-TEMPERATURE/CELL VOLTAGE, NO LOAD

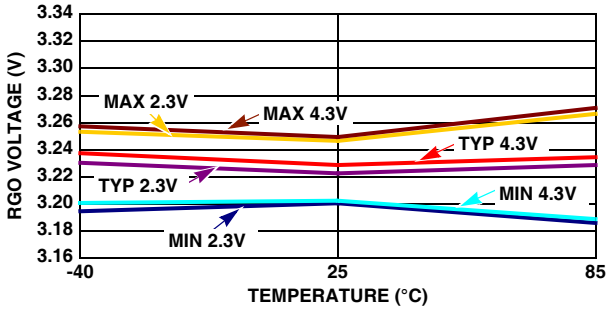


FIGURE 7. RGO REGULATION OVER-TEMPERATURE/CELL VOLTAGE, 35mA LOAD (350µA RGC CURRENT, NPN GAIN = 100)

WKUP Pin Operation

The microcontroller can easily put the ISL9217 to sleep by writing 80H to the ISL9217 Register 4, since going to sleep does not turn off any critical pack power supply. Once the ISL9217 is asleep, the microcontroller can wake the ISL9217 by writing a 40H to the ISL9216 Register 2. This sets the WKUPR bit in the ISL9216, which pulls the ISL9217 pin low, waking the device.

The ISL9216 sleep conditions are a little more complicated. Once the microcontroller puts the ISL9216 to sleep, there are two ways to wake it up again (without power cycling the device). One way uses the WKUP pin in an active LOW mode. The other uses the WKUP pin in an active HIGH mode.

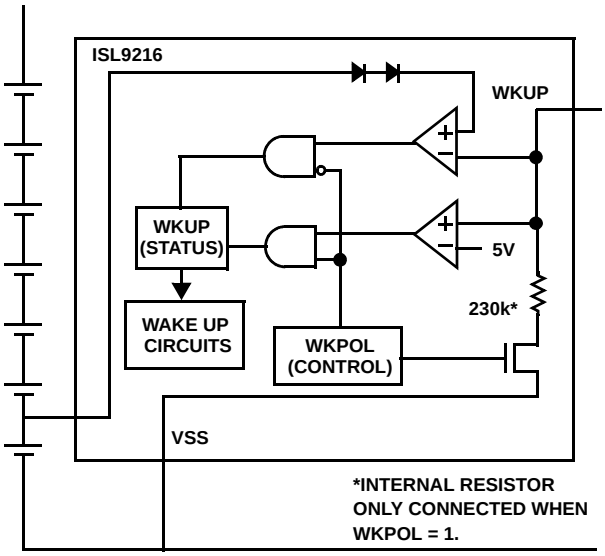


FIGURE 8. WAKE UP CONTROL CIRCUITS

In an active LOW connection (WKPOL bit = '0' - default), the device wakes up by connecting a charger to the pack. (See Figure 8). In this case a pack requires only two terminals (Pack+ and Pack-). No additional terminals are needed on the pack for wake up.

In this mode, when the pack is asleep, the FETs are off and the WKUP pin is pulled high with a resistor external to the ISL9216. Connecting the pack to a charger creates a voltage divider, which pulls the WKUP pin low. When the WKUP pin voltage goes below the WKUP threshold, the ISL9216 wakes up and turns on the 3.3V voltage regulator. (See "Active LOW WKUP Pin Operation" on page 6 for more details).

In an active HIGH configuration (WKPOL = '1'), the device wakes up when either the load or a charger is connected to the pack, but this configuration requires an extra pack terminal to operate.

In this mode, the WKUP pin connects through a resistor and an additional pack terminal to the PACK+ terminal outside the pack (see Figure 10). The resistor, combined with a resistor internal to the ISL9216, forms a resistor divider. When a charger or load connects to the pack, the divider pulls the voltage at the WKUP pin high and wakes up the pack. With no tool or charger connected, the internal resistor pulls WKUP low to prevent the pack from waking up inadvertently. See "Active HIGH WKUP Pin Operation" on page 7 for more details.

Active LOW WKUP Pin Operation

When the ISL9216 devices use the WKUP pin in the active LOW (default) mode, the WKUP pin threshold is normally set such that a fully charged pack can still be waken by a charger supplying the regulated charge voltage. For example, for a 12-cell pack in sleep mode, the fully charged pack voltage is 50.4V. The wake up level should be set such that a charger with a regulated 50.4V output wakes the pack.

The recommended external connection of the WKUP pin is shown in Figure 9. The R_3 resistor is needed to prevent the WKUP voltage from going above the ISL9216 VCC voltage when the FETs turn off. The resistor divider should keep the WKUP below the ISL9216 VCC voltage and also keep it above the WKUP negative edge threshold level.

The resistors needed for the recommended wake-up threshold are calculated (approximately) as follows:

$$V_{WKUP2}(min) > \frac{R_2}{R_1 + R_2} \times CELLmax \times N \quad \text{(EQ. 2)}$$

where N is the number of cells in the pack, and V_{WKUP2}(min) is calculated at the maximum cell voltage.

In selecting resistors, first choose the R_1 value as the highest value that is reasonable to use, since this primarily determines the current consumption of this circuit. Then calculate the value for R_2. The actual value of R_2 chosen should be smaller than the value calculated.

The value of the chosen R_2 resistor is not too critical, since the WKUP voltage should go well above the WKUP falling edge threshold level when the ISL9216 is in the sleep mode and the FETs are off. So, an R_2 that is much smaller than the calculated value would be fine with the understanding that a lower resistance value will draw more current. It is best to use the largest value for R_2 that does not exceed the calculated value.

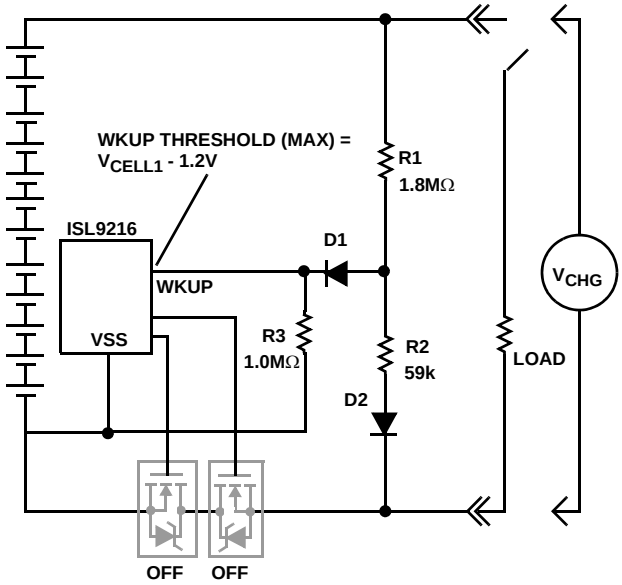


FIGURE 9. SETTING THE THRESHOLD FOR THE ISL9216 ACTIVE LOW WKUP PIN (WKPOL = LOW)

As shown in Figure 9, the voltage at the WKUP pin with no charger connected and the power FETs off is about a third of the pack voltage. This is below the ISL9216 VCC voltage but well above the wake up falling edge threshold. Connection of the pack to the charger with the power FETs off causes the voltage on the WKUP pin to drop below the input threshold and the ISL9216 wakes up.

The values are calculated with a full pack, because this is the worst case condition. When a charger is connected to a pack that is in sleep mode due to low voltage cells, the voltage on the VMON pin will go well below GND without the use of Diode D_1, which is required to prevent this condition. Diode D_2 is an optional diode to prevent higher leakage current from the cells with a load connected and the power FETs off.

Use Equation 3 (for the circuit shown in Figure 9) to determine the minimum unloaded voltage necessary from the charger to wake a fully charged pack, using the resistors previously calculated.

$$(CellV(max) \times N - V_{WKUP2}min) \times \frac{R_2 + R_1}{R_1} = V_{charger} \quad \text{(EQ. 3)}$$

where N is the number of cells in the pack.

For a 12-cell pack, the charger voltage needs to be at least 50.31V to wake a fully charged pack (Pack voltage = 50.4V).

In this active low configuration, the pack cannot detect the presence of a load when in sleep mode. Instead, the pack wakes up only when the charger is connected to the pack.

Active HIGH WKUP Pin Operation

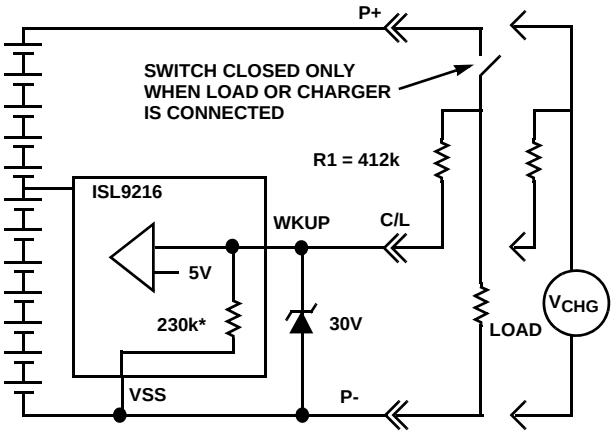
When the ISL9216 uses the WKUP pin in the active HIGH mode, the external resistor needed to select the proper wake-up threshold is shown in Figure 10 and Equation 4 is used for setting the value:

$$R_1 < \left[\frac{CellV(min) \times Numcells}{V_{WKUP1}(max)} - 1\right] \times R_{WKUP}(min) \quad \text{(EQ. 4)}$$

Assuming a 12-cell pack and a minimum cell voltage of 2.3V, a minimum internal resistance (R_{WKUP}) of 130kΩ (from the data sheet FN6488) and a WKUP threshold of 6.6V (0.1V above the max threshold in the data sheet), the Equation for R_1 is:

$$R_1 < \left[\frac{2.3 \times 12}{6.6} - 1\right] \times 130k = 413.6k\Omega \quad \text{(EQ. 5)}$$

The zener diode in the circuit of Figure 10 is required to prevent voltages on the WKUP pin that exceed the absolute maximum VCC voltage in the event the switch is closed and the microcontroller sets the WKPOL bit to “0”.



*** INTERNAL RESISTOR ONLY CONNECTED WHEN WKPOL = 1.**

FIGURE 10. SETTING THE THRESHOLD FOR THE ISL9216 ACTIVE HIGH WKUP PIN (WKPOL = HIGH)

Power Path Connections

The ISL9216 controls pack operation through one, two, or three power FETs on the negative terminal of the pack. The power FETs can connection two basic different ways, a single charge/discharge path and separate charge and discharge paths.

Single Charge/Discharge Path

The most common connection of power path FETs is to use both a charge and discharge FET and a single charge/discharge path. In this connection, back-to-back FETs provide both discharge and charge protection for the pack (See Figure11). In this way, any “out of bounds” condition in the pack cause the cells in the pack to be isolated from external conditions.

The DFET output of the ISL9216 actively controls both the turn on and turn off of the discharge FET. When the microcontroller sets the DFET bit in the ISL9216, the ISL9216 outputs a current to the gate of the DFET causing the gate to charge up. When the gate voltage reaches the FET turn on threshold, the FET turns on. The ISL9216 continues to output the turn on current until the voltage reaches the VCELL3 voltage. It is clamped at this level.

When the ISL9216 turns off the DFET, either as a result of a protection mechanism, or under microcontroller control, the ISL9216 pulls the DFET gate low with a high current (>100mA). This turns off the FET very fast.

The CFET output of the ISL9216 actively turns the charge FET on (the same as the DFET output) but the ISL9216 relies on an external resistor to turn off the FET (see Figure11). This is because the charge FET V_{GS} voltage may go well below the ISL9216 ground voltage when connected to a charger, preventing the ISL9216 from supplying the voltage necessary to turn the FET off. The selection of the charge FET resistor is determined by the C_{gs} capacitance of the FET and how fast the charge FET needs to turn off. This resistor also cannot be so

small that it clamps the FET gate voltage below the FET turn on threshold. For example, the output current of the ISL9216 CFET pin is 80µA minimum. For a FET with a V_{GS} of 3V, R_1 needs to be at least 37.5kΩ or the FET may never turn on.

Figure 11 shows the two FETs being used in a single path. It also shows a sense resistor being used for current monitoring of both discharge and charge current. Because the sense resistor is the same for both charge and discharge, the ratio of the charge overcurrent limits and the charge short circuit limits is primarily determined by the internal threshold settings, however an external resistor divider can provide more flexibility in some situations (see “Current Sense Resistor” on page 10).

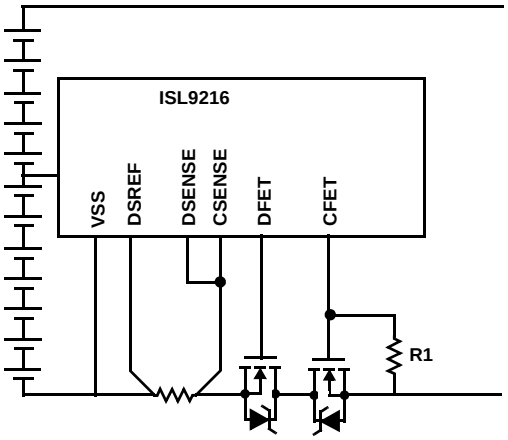


FIGURE 11. BACK-TO-BACK POWER FETS IN SINGLE CHARGE/DISCHARGE PATH

An optional single path connection uses only the discharge FET for pack protection. This connection assumes that the external charger protects the cells in the pack from an over charge condition, since the pack electronics will not be able to stop the charge. To do this, the charger communicates with the pack during the charge operation. During this communication, the cell voltages are passed to the charger. These cell voltages become part of the charger over charge limit algorithm.

The major advantages of using the single FET are:

- More of the cell voltage is applied directly to the load resulting in less power loss in the pack.
- It is less costly to use the single FET, especially in high current applications where it may be necessary to parallel the power FETs to achieve the necessary current handling capability of the pack.
- This configuration allows the pack to be charged, even if the cell voltages drop too low for the ISL9216 to remain powered.

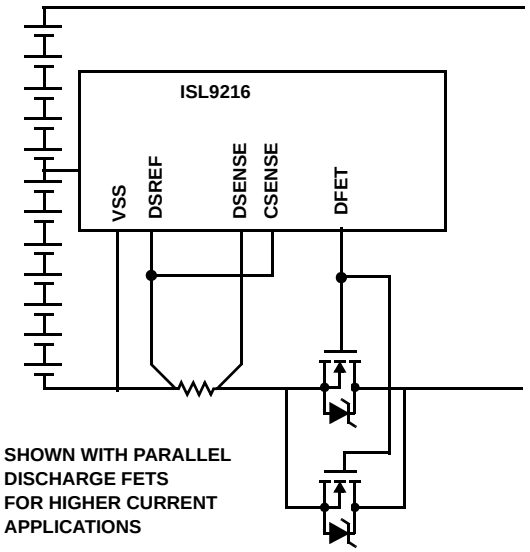


FIGURE 12. DISCHARGE POWER FET ONLY IN SINGLE CHARGE/DISCHARGE PATH

Separate Charge/Discharge Path

Another method of connecting the power FETs is to provide separate charge and discharge paths. This is shown in Figure 13. In this case, the pack requires only a single discharge FET (Q_1), but requires “back-to-back” charge FETs (Q_2 and Q_3). The charge path needs both FETs because without Q_2, the Q_3 body diode creates a discharge path, even if the discharge FET is off. This can present a safety hazard for the pack.

By designing a separate charge and discharge path, the current sense elements can be different sizes, so the overcurrent threshold limits are better able to meet the application requirements. Also, since the peak charge current is usually much lower than the peak discharge current, the size (and cost) of the charge FETs can be much less.

Problems with this connection concern space and cost. Even though smaller FETs can be used for the charge connection, two FETs generally still cost more than one FET and take more board space. This coupled with the need for an additional pin on the pack and the possibility of having to parallel the discharge FET, makes this a more costly, if more flexible, solution.

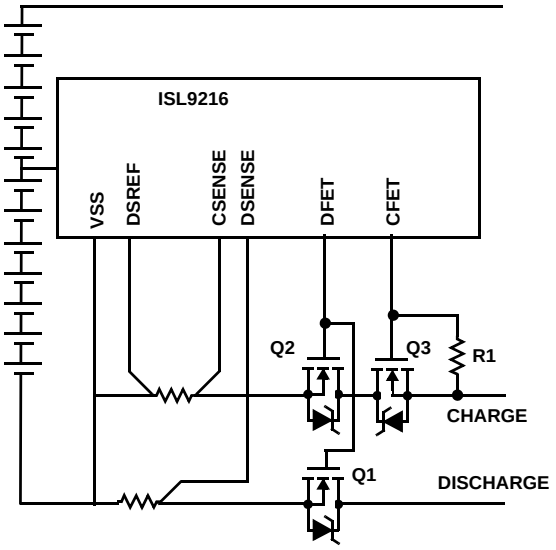


FIGURE 13. POWER FETS IN A SEPARATE CHARGE/DISCHARGE PATH CONNECTION

Protection Functions

In the default condition, the ISL9216 automatically responds to discharge overcurrent, discharge short circuit, charge overcurrent, internal over-temperature and external over-temperature conditions. These functions are described in more detail in the following, starting with current protection mechanisms.

Overcurrent Protection Functions

The ISL9216 continually monitors the charge current and discharge current by monitoring the voltage at the CSENSE and DSENSE pins (respectively). If either voltage exceeds a selected value for a time exceeding a selected delay, then the device enters an overcurrent or short circuit protection mode. In these modes, the device automatically turns off both power FETs and hence prevents current from flowing through the terminals P+ and P-.

The voltage thresholds and the response times for discharge overcurrent, charge overcurrent, and discharge short circuit conditions are each selected by bits in a control register. In the default condition, the bits are generally set to the safest state. In this condition, the FETs are off, the overcurrent and short circuit settings are at the minimum threshold level and the short circuit setting has the minimum time delay.

See Table 1 and Table 2 for threshold and timing options. The power-up condition for all registers is “0”.

After the ISL9216 detects any overcurrent condition, and both power FETs are turned off, the ISL9216 sets a status flag. A discharge overcurrent condition sets the DOC bit, a charge overcurrent condition sets the COC bit, and a discharge short circuit condition sets the DSC bit. (When the FETs turn off, the DFET and CFET bits also reset to zero).

TABLE 1. OVERCURRENT VOLTAGE THRESHOLD SETTINGS

REGISTER 5		
BIT 6 OCDV1	**BIT 5 OCDV0**	**OVERCURRENT DISCHARGE VOLTAGE THRESHOLD**
0	0	V_{OCD} = 0.10V
0	1	V_{OCD} = 0.12V
1	0	V_{OCD} = 0.14V
1	1	V_{OCD} = 0.16V
BIT 3 SCDV1	**BIT 2 SCDV0**	**SHORT CIRCUIT DISCHARGE VOLTAGE THRESHOLD**
0	0	V_{SCD} = 0.20V
0	1	V_{SCD} = 0.35V
1	0	V_{SCD} = 0.65V
1	1	V_{SCD} = 1.20V
REGISTER 6		
BIT 6 OCCV1	**BIT 5 OCCV0**	**OVERCURRENT CHARGE VOLTAGE THRESHOLD**
0	0	V_{OCD} = 0.10V
0	1	V_{OCD} = 0.12V
1	0	V_{OCD} = 0.14V
1	1	V_{OCD} = 0.16V

TABLE 2. OVERCURRENT DELAY TIME SETTINGS

REGISTER 5		
BIT 1 OCDT1	**BIT 0 OCDT0**	**OVERCURRENT DISCHARGE TIME-OUT**
0	0	t_{OCD} = 160ms (2.5ms if DTDIV = 1)
0	1	t_{OCD} = 320ms (5ms if DTDIV = 1)
1	0	t_{OCD} = 640ms (10ms if DTDIV = 1)
1	1	t_{OCD} = 1200ms (20ms if DTDIV = 1)
REGISTER 6		
Bit 1 OCCT1	**Bit 0 OCCT0**	**OVERCURRENT CHARGE TIME-OUT**
0	0	t_{OCC} = 80ms (2.5ms if CTDIV = 1)
0	1	t_{OCC} = 160ms (5ms if CTDIV = 1)
1	0	t_{OCC} = 320ms (10ms if CTDIV = 1)
1	1	t_{OCC} = 640ms (20ms if CTDIV = 1)
Bit 4	SCLONG Short circuit long delay	When this bit is set to ‘0’, a short circuit needs to be in effect for 190µs before a shutdown begins. When this bit is set to ‘1’, a short circuit needs to be in effect for 10ms before a shutdown begins.
Bit 3	CTDIV Divide charge time by 32	When set to “1”, the charge overcurrent delay time is divided by 32. When set to “0”, the charge overcurrent delay time is divided by 1.
Bit 2	DTDIV Divide discharge time by 64	When set to “1”, the discharge overcurrent delay time is divided by 64. When set to “0”, the discharge overcurrent delay time is divided by 1.

Current Monitoring

The ISL9216 monitors the current by comparing the voltage at the CSENSE or DSENSE pins relative to an internal threshold level. An external circuit generates a voltage from the current. Several methods are available for establishing this current limit threshold. These include using a sense resistor, a sense FET, and techniques for translating the FET $r_{DS(ON)}$.

A battery pack with a single charge/discharge path uses the same element to monitor the two different levels of current encountered in an overcurrent condition and a short circuit condition. When designing the current sense circuit, use the setting in Table 3 to pick a setting in which the ratio between the short circuit and overcurrent thresholds most closely matches the desired ratio. (These ratios are shown graphically in Figure 14). This determines the settings for the ISL9216 discharge thresholds.

TABLE 3. SHORT CIRCUIT TO OVERCURRENT RATIOS

SETTING	SHORT CIRCUIT THRESHOLD	OVERCURRENT THRESHOLD	RATIO
1	1.20V	0.10V	12.0
2	1.20V	0.12V	10.0
3	1.20V	0.14V	8.6
4	1.20V	0.16V	7.5
5	0.65V	0.10V	6.5
6	0.65V	0.12V	5.4
7	0.65V	0.14V	4.6
8	0.65V	0.16V	4.1
9	0.35V	0.10V	3.5
10	0.35V	0.12V	2.9
11	0.35V	0.14V	2.5
12	0.35V	0.16V	2.2
13	0.2V	0.10V	2.0
14	0.2V	0.12V	1.7
15	0.2V	0.14V	1.4
16	0.2V	0.16V	1.3

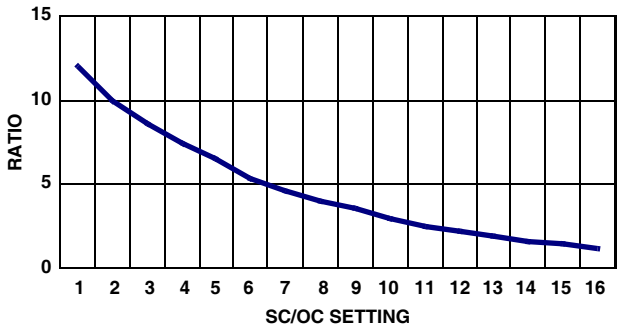


FIGURE 14. SHORT CIRCUIT TO OVERCURRENT RATIO

Current Sense Elements

CURRENT SENSE RESISTOR

Sense resistors (Figure 15) are the easiest and most flexible method of monitoring current in the charge or discharge path (or both). This is a relatively accurate solution, but has some limitations. An application with high current limits will likely require the use of high power sense resistor. These can be expensive and will generate heat in the pack. Also, a sense resistor can introduce significant voltage drop and power loss to the load.

In the simplest solution a sense resistor is used for a relatively low current application (See Example 1). In this solution, first select the thresholds and external sense resistor for a pack by using Table 3 to select the closest ratio to the desired short circuit/overcurrent ratio. Use the settings in the table to select the overcurrent and short circuit current thresholds. Next, select a sense resistor that provides the selected overcurrent threshold at the desired current limit. From this, verify the short circuit limit.

Example 1: Designing discharge current limits.

Using the circuit of Figure 11.

Desired Short Circuit Current Level: 15A
Desired Overcurrent Level: 5A
Ratio (SC/OC): 3.0

Choose Table setting 10: 2.9
Short circuit threshold = 0.35V
Overcurrent threshold = 0.12V

Pick a sense resistor of 0.12V/5A = ~0.025Ω.

Results:
Overcurrent threshold = 4.8A
Short circuit threshold = 14A.
Overcurrent (charge) options: 4A, 4.8A, 5.6A, 6.4A.

With a single charge/discharge path, there are not many options for charge and discharge current limits, since the same resistor is used for both charge and discharge. If the current limits are small enough, the following external circuit can give some flexibility to the pack design (See Figure 15).

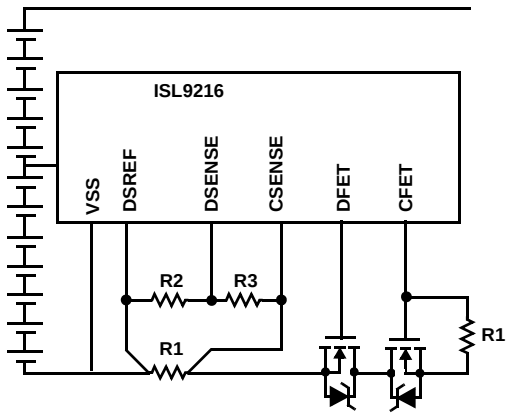


FIGURE 15. USING A RESISTOR DIVIDER TO SELECT CHARGE AND DISCHARGE OVERCURRENT LEVELS

In this case, select the sense resistor for the lower of the charge and discharge current limits. The sense resistor provides the voltage for this lower limit. Then, the resistor divider provides the other limits.

While the technique in Example 2 provides a flexible method of addressing the charge and discharge overcurrent settings, it has a limitation. This method requires the use of a larger sense resistor to provide for the use of the voltage divider. In higher current applications this can be a significant drawback. Consider Example 2, which does not include the resistor divider, but shows the consequences of using a sense resistor in a high current design.

Example 2: Designing discharge and charge current limits using a sense resistor and resistor divider.

Using the circuit of Figure 15.

Desired Short Circuit Current Level:	15A
Desired Overcurrent Level (discharge):	5A
Desired Overcurrent (charge):	2A
Ratio (SC/OC):	3.0
Choose lowest charge Overcurrent threshold:	0.1V
Choose sense resistor:	0.05Ω

Determine the short circuit to overcurrent ratio:
Choose Table setting 10: 2.9
Short circuit threshold = 0.35V
Overcurrent threshold = 0.12V

Pick a resistor divider of (2A/5A)*(0.12/0.1) = 0.48.
Select the divider resistors:

$$\frac{R_2}{R_2 + R_3} = 0.48 \quad \text{(EQ. 6)}$$

R_2 = 96kΩ
R_3 = 104kΩ

Results:

Overcurrent threshold (charge) =	2A
Overcurrent threshold (discharge) =	5A
Short circuit threshold =	14.6A

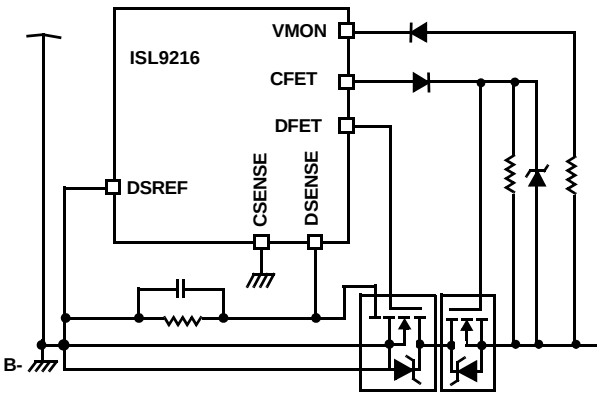


FIGURE 16. MEASURING CURRENT WITH A SENSE FET

Example 3: Using a sense resistor in a high current application.

Desired Short Circuit Current Level:	120A
Desired Overcurrent Level:	20A
Ratio (SC/OC):	6.0
Choose Table setting 10:	6.5

Short circuit threshold = 0.65V
Overcurrent threshold = 0.1V

Pick a sense resistor of 0.1V/20A = ~0.005Ω.

Results:
Overcurrent threshold = 20A
Short circuit threshold = 130A.

Power dissipation in resistor at 20A: 2W
(could be continuous)
Select 5Ω resistor to minimize heating.
Power dissipation at 120A: 72W
(until S.C. shutdown)

SENSE FET

As shown in Figure 16, the sense resistor is replaced by a resistor in the sense path of a special type of FET called a sense FET. Sense FETs provide two additional pins. One of these provides a “Kelvin” connection to the FET source to get a low current reference path. The second connection provides an output current proportional to the load current. One type of sense FET provides a sense current that is about 2600x lower than the load current.

In dealing with relatively high current applications, the sense FET has several advantages over a sense resistor. There is no power loss across the sense resistor, improving the efficiency of the pack. There is no heating of the pack due to the sense resistor. There is more flexibility in the setting of the overcurrent threshold because the resistor in the sense lead is much higher resistance. Using a sense FET may be less expensive than a sense resistor because the additional cost of a sense FET may be more than offset by not using a large wattage sense resistor.

Using a sense FET allows somewhat higher power applications to be considered. For example, using a 6Ω resistor in the sense lead of a sense FET above allows the designer to set an overcurrent threshold of 45A and short circuit threshold of 450A. These are limits that make sense resistors somewhat impractical.

The most significant drawbacks of using a sense FET is that there are relatively few choices of devices. They should be matched with a non-sense FET for a “back-to-back” pair and they cannot be used to measure the charge current.

FET DESATURATION

This technique uses changes in the discharge FET $r_{DS(ON)}$ as the power dissipation increases to detect an overcurrent condition and turn off the pack discharge.

As shown in Figure 17, the sense resistor is replaced by a diode (or two diodes, in order to get the voltage at point A to about 1V above the FET drain to source voltage) and three resistors.

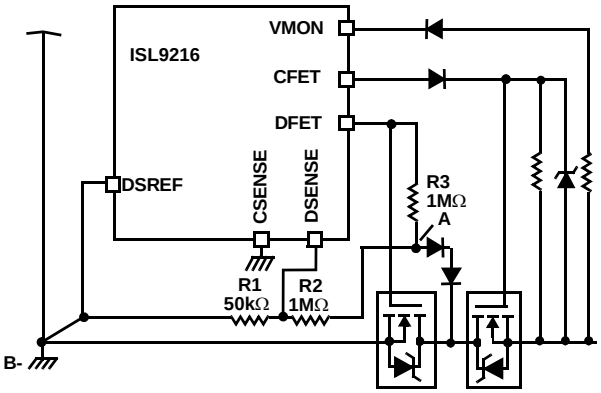


FIGURE 17. MEASURING CURRENT USING FET DESATURATION

A more complete analysis of this solution is planned for another application note, but some guidelines for designing this circuit follow.

The value of R_3 must be fairly large, because internal to the ISL9216 is a 5kΩ resistance from VCELL3 to the DFET pin. If R_3 is too small, the voltage at the DFET pin could drop significantly.

The R_1 and R_2 series resistance also needs to be fairly large. The recommendation is that this resistance be greater than 1MΩ. The reason for this is to allow for the largest swing of voltage across the discharge FET. The maximum voltage at point P is set by the resistor divider formed by R_3 and (R_1 + R_2). With the values in Figure 17, the maximum voltage at point A, with a minimum cell voltage of 2.3V, is 4.5V. With a 1.2V drop across the diode, the maximum drain source voltage (V_{DS}) that can be monitored is 3.3V. This can be increased a little by reducing the diode drop.

Though not shown in Figure 17, it is also be possible to detect a charge overcurrent condition using this circuit. By adding a transistor and some resistors, an inverter can be built that changes the polarity of the voltage at point A. This can then be divided and connected to the CSENSE pin. This needs to be designed so it does not load the DFET output or effect the performance of the discharge sense circuit.

This method of overcurrent protection has a number of advantages. First, it does not use a sense resistor in series with the discharge path. This allows more power to be applied to the load, instead of being burned in the sense resistor. The diode and three resistors are also a very cost effective replacement for an often very expensive sense resistor.

The voltage at point A can be monitored by the microcontroller to get a representation of the pack current (both charge and discharge). This may not be accurate enough to be used for coulomb counting, but it is useful for detecting the presence of charge and discharge currents. The designer can use this knowledge to build in power management routines, create automatic cell balance algorithms, and make decisions about pack shutdown operations.

This overcurrent circuit is also adaptive and shuts down the pack earlier if the FET heats up, regardless of the pack current. This situation might occur under the following conditions:

- A long period of high current (but not overcurrent) is applied to the load, as might be the case if a motor stalls.
- The repeated cycling of the load causing current surges that heat the FET.
- As the FET heats, the $r_{DS(ON)}$ increases, accelerating further FET heating. This can happen even without an increase in load current.
- When the pack is supplying a large load when the pack capacity is low, the high current spikes could periodically and for short durations drop the cell voltages to 2.3V (or less). This drops the FET gate voltage to less than 6.8V. At this lower gate voltage, the $r_{DS(ON)}$ increases.

If these conditions go on long enough, in a system using a sense resistor, the FET can fail even though the current never reached the shutdown threshold.

The main limitation of this technique is that the $r_{DS(ON)}$ of the FET can vary over a relatively wide range. So, designing this circuit will be a trade-off between protecting the internal components and providing maximum power to the load.

Another approach to the same technique is to use a small FET in parallel with the power FET and divide the voltage to get an overcurrent level. This has some advantages over the previous version, i.e. it does not load the DFET output and it allows monitoring a higher drain to source voltage. But, it is probably a more expensive solution and the voltage during charge is negative, so is not useful for monitoring with the microcontroller.

Over-riding Automatic Overcurrent Response

An alternative method of providing the protection function, if desired by the designer, is to turn off the individual automatic safety responses. See Table 4 for control bits that turn off the automatic control. In this case, the ISL9216 device still monitors the conditions and sets the status bits, but it takes no action in overcurrent or short circuit conditions. Safety of the pack depends instead on the microcontroller to send commands to the ISL9216 to turn off the FETs.

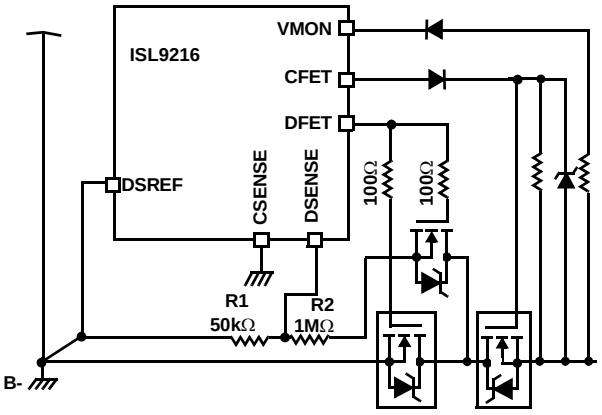


FIGURE 18. MEASURING CURRENT USING FET DESATURATION (ALTERNATE APPROACH)

TABLE 4. AUTOMATIC CURRENT RESPONSE OVER-RIDE SETTINGS

REGISTER 5		
Bit 7	DENOCD Turn off automatic OC discharge control	When set to ‘0’, a discharge overcurrent condition automatically turns off the FETs. When set to ‘1’, a discharge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the DOC bit, which also turns on the TEMP3V output.
Bit 4	DENSCD Turn off automatic SC discharge control	When set to ‘0’, a discharge short circuit condition turns off the FETs. When set to ‘1’, a discharge short circuit condition will not automatically turn off the FETs. In either case, the condition sets the SCD bit, which also turns on the TEMP3V output.
REGISTER 6		
Bit 7	DENOCC Turn off automatic OC charge control	When set to ‘0’, a charge overcurrent condition automatically turns off the FETs. When set to ‘1’, a charge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the COC bit, which also turns on the TEMP3V output.

To facilitate a microcontroller response to an overcurrent condition (especially if the microcontroller is in a low power state), the charge overcurrent flag (COC), discharge overcurrent flag (DOC), or short circuit flag (DSC) being set causes the ISL9216 TEMP3V output to turn on and pull high. (See Figure 20 on page 15). This output can be used as an external interrupt by the microcontroller to wake-up quickly to handle the overcurrent condition.

When an overcurrent or short circuit condition occurs and the delay time elapsed, the DSC, DOC, or COC bits are set in the Status register (addr: 01H).

One way to use these status bits is to design the system such that the microcontroller is in a sleep state to conserve power. It uses both a timer and the TEMP3V input as interrupt sources. The microcontroller periodically wakes up to monitor the cells and goes back to sleep. In an “emergency” overcurrent condition, the microcontroller wakes up in response to the TEMP3V interrupt and turns off the FETs.

In practice, when any of the three overcurrent status bits are set, the TEMP3V output turns on and does two things.

1. This turns on the ISL9216 external over-temperature monitor circuit. (There is no harm in turning this on too often, except that the circuit consumes about 400µA of current until TEMP3V turns off).
2. If the microcontroller is in a sleep mode, TEMP3V wakes up the microcontroller by applying a voltage to the interrupt. When the microcontroller services the interrupt, it reads the status register to determine if there was an overcurrent or short circuit condition. Reading the status register resets the status bits, which turns off the TEMP3V output.

If the microcontroller is not in the sleep mode, the microcontroller can disable the TEMP3V interrupt so that a TEMP3V input does not disrupt other code, or it can leave the interrupt on to provide the microcontroller a hardware response to an overcurrent condition. If the interrupt is left on, then reading the external temperature with the AO3:AO0 bits also causes an interrupt to the microcontroller. But a simple scan of the status register indicates whether this was an overcurrent condition, or a normal temperature scan.

Load Monitoring

Once the power FETs turn off as a result of an overcurrent condition, they are not automatically turned back on by the ISL9216. They are turned on again by the external microcontroller. The microcontroller can turn on the FETs right away, but if the load or short circuit is still present, there will be a big current surge through the FETs. If this turn-off and
turn-on oscillation is not controlled, then the FETs can heat and possibly fail. So, before the microcontroller turns on the power FETs after an overcurrent condition, it is best to check to see if the load has been removed before turning the FETs on again.

DISCHARGE LOAD MONITORING

For pack discharge conditions, the ISL9216 provides a mechanism for detecting the removal of the load from the pack following an overcurrent or short circuit condition. This is called the load monitor and uses the VMON pin on the ISL9216.

The load monitor function is normally not active to minimize current consumption. To use it, the circuit must be activated by the microcontroller. It works by internally connecting the VMON pin to VSS with a current sink circuit. This internal sink and the external load form a voltage divider with the VMON pin reflecting the divided voltage. The VMON pin is compared to an internal reference. If VMON is above the

reference, then the pack load is still present. If the voltage at VMON is below the threshold, then the load has been released enough to allow the power FETs to be turned on again. The circuit operates as shown in Figure 19.

In operation, when an overcurrent or short circuit event happens, the DFET and CFET turn off. At this time, the R_L resistance is small and the load monitor is off. As such, the voltage at P- rises to nearly the pack voltage. The external diode D_4, in conjunction with resistor R_1 clamps the VMON pin to 30V to protect the input. Diode D_4 also protects the input in the event a severely undercharged pack is connected to a charger. The ISL9216 handles up to -22V on VMON, but in a 12-cell pack with cell voltages of 2V each, a 50.4V charger would generate -26V on the VMON pin without the D_4 diode.

Once the power FET turns off, the microcontroller activates the load monitor by setting the LDMONEN bit. This turns on a FET that adds a pull down resistor to the load monitor circuit. While still in the overload condition the combination of the load resistor, an external adjustment resistor (R_1), and the internal load monitor resistor form a voltage divider. R_1 is chosen so that when the load is released to a sufficient level, the LDFAIL condition resets.

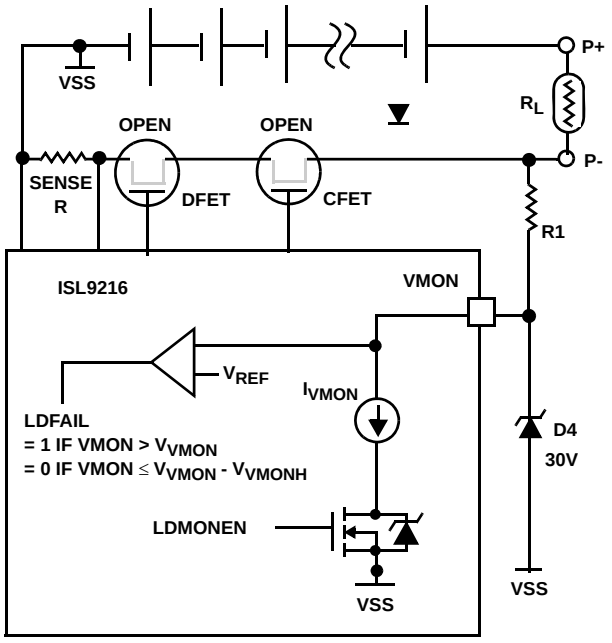


FIGURE 19. LOAD MONITOR CIRCUIT

Load Monitor Example:

Removing an overcurrent or short circuit condition results in the value of R_L increasing. To determine where the load monitor detects the release of the load and to set the value of R_1, use Equation 7:

$$R_L + R_1 \geq \frac{(\text{CellV} \times \text{Numcells}) - V_{VMON}(\text{min})}{I_{VMON}(\text{max})} \quad \text{(EQ. 7)}$$

For a twelve cell pack, the minimum combined resistance at a pack voltage of 29.4V is:

$$R_L + R_1 = \frac{50.4 - 1.1\text{V}}{60\mu\text{A}} = 822\text{k}\Omega \quad \text{(EQ. 8)}$$

At a depleted pack voltage of 2.5V per cell, P+ is 30V and the $R_L + R_1$ resistance is 482kΩ. So, in this case, if R_1 is set to 450kΩ, the load resistance must exceed 32kΩ to recover from an overcurrent when the pack is depleted, and exceed 372kΩ when the pack is fully charged.

At the opposite extreme (based on ISL9216 parameter variations):

$$R_L + R_1 \geq \frac{(\text{CellV} \times \text{Numcells}) - V_{VMON}(\text{min})}{I_{VMON}(\text{min})} \quad \text{(EQ. 9)}$$

$$R_L + R_1 = \frac{50.4 - 1.1\text{V}}{20\mu\text{A}} = 2.47\text{M}\Omega \quad \text{(EQ. 10)}$$

The $R_L + R_1$ for a fully depleted pack 1.45MΩ. These values are summarized in the Table 5.

TABLE 5. $R_L + R_1$ OVERCURRENT RECOVERY RESISTANCE

RL + R1	FULLY CHARGED PACK	FULLY DEPLETED PACK
Max VMON current	822kΩ	482kΩ
Min VMON current	2.47MΩ	1.45MΩ

Table 5 shows that, in effect, the load needs to be completely removed before the circuit recovers. For an R_1 of 450kΩ, the load needs to exceed 2MΩ in the worst case condition.

CHARGE LOAD MONITORING

The ISL9216 load monitor circuit does not provide detection of charger removal after a charge overcurrent condition, because it is likely that the voltage on the charger will be higher than the pack voltage and the VMON pin would go negative.

In the event that the pack FETs turn off due to an overcurrent condition during charge, the microcontroller will need to use a timing based procedure for turning the FETs on again. The recommended procedure for responding to a charge overcurrent is to wait for a period of time, then turn the FETs on again. This delay time is dependent on the choice of FETs and its power handling capabilities. The time should be set long enough for the FET to cool off.

After the FET turns back on, if another charge overcurrent happens within a fixed time period, then the microcontroller might decide to wait much longer before turning the FETs on or it might keep the FETs off (effectively disabling the pack). Repetitive overcurrent conditions during charge could indicate a pack failure, charger failure, or the use of the wrong pack/charger combination. The specific algorithm requirements are up to the pack/system designer.

Over-Temperature Safety Functions

EXTERNAL TEMPERATURE MONITORING

The external temperature is monitored by using a voltage divider consisting of a fixed resistor and a thermistor. This divider is powered by the ISL9216 TEMP3V output. This output is normally controlled so it is on for only short periods to minimize current consumption.

Without microcontroller intervention, the ISL9216 continuously turns on TEMP3V output (and the external temperature monitor) for 4ms every 512ms. In this way, the external temperature is monitored even if the microcontroller is asleep. If the ATMPOFF bit is set, this automatic temperature scan is turned off.

The TEMP3V pin turns on when the microcontroller sets the AO3:AO0 bits to select that the external temperature voltage be placed AO. As long as the AO3:AO0 bits point to the external temperature the TEMP3V output remains on.

The microcontroller can over-ride both the automatic temperature scan or the microcontroller controlled temperature scan by setting the TEMP3ON configuration bit. This turns the TEMP3V output on all the time to keep the temperature control voltage on indefinitely. This will consume a significant amount of current, so it is likely this feature would be used for special or test purposes.

When the TEMP3V output is on, the external temperature voltage is compared with an internal voltage divider that is set to TEMP3V/13. When the voltage is below this threshold for more than 1ms, the external temperature fail condition exists.

To set the external over-temperature limit, determine the resistance of the desired thermistor at the temperature limit. Then, select a fixed resistor that is 12x that value.

Example 4: Selecting the resistor/thermistor for external over-temperature limit.

Selected Thermistor:	MuRata XH series
Desired Over-temperature Limit:	+55°C
Thermistor resistance at limit:	3.54kΩ

Calculate R_X value (see Figure 20):

3.54kΩ * 12 = 42.48kΩ

Pick an R_X resistor: 42.2kΩ

Results:
Calculated temperature threshold: 42.2kΩ/12 = 3.517V
Temperature limit (MuRata table look up): +55.17°C

PROTECTION

When the ISL9216 detects an internal or external over-temperature condition, the FETs are turned off, the cell balancing function is disabled, and the IOT bit or XOT bit (respectively) is set.

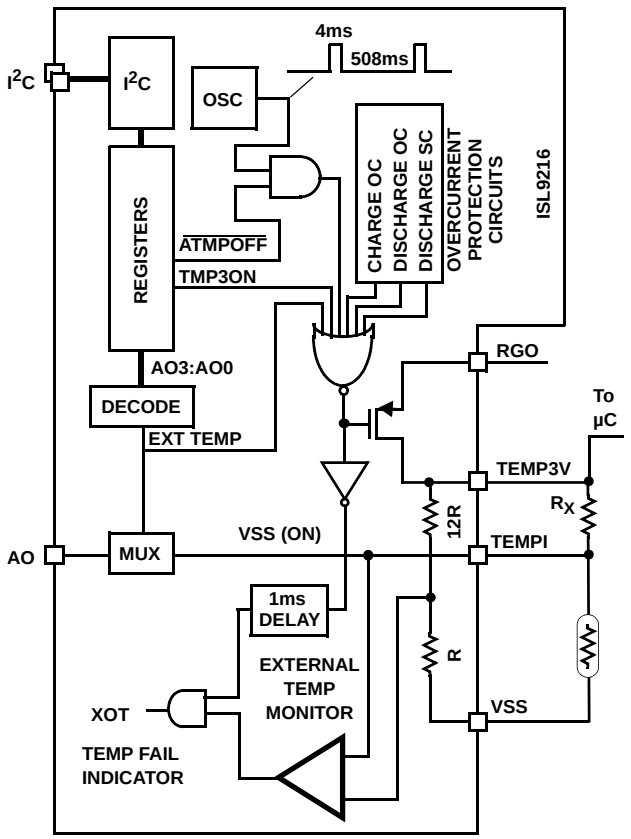


FIGURE 20. EXTERNAL TEMPERATURE MONITORING AND CONTROL (ISL9216 ONLY)

While in an over-temperature condition, the ISL9216, ISL9217 prevents cell balancing and the power FETs are held off. This continues until the temperature drops back below the temperature recovery threshold. During a temperature shutdown, the microcontroller can monitor the internal temperature through the analog output pin (AO), but any writes to the CFET bit, DFET bit, or cell balancing bits are ignored.

The automatic response for the ISL9216, ISL9217 was chosen to prevent damage to the IC, the cells, and the pack. If the internal temperature reaches the internal temperature limit, it is most likely due to heating from cell balancing, perhaps as a result of a faulty microcontroller or runaway code. Keeping the cell balance resistors on when the ISL9216, ISL9217 internal temperature is above the threshold temperature is not advised.

If the ISL9216 detects the external temperature is reaching its limit, it is possible that the cells are over heating due to a fast charge or discharge. The external temperature protection circuit turns the power FETs off to prevent further heating, which can lead to thermal runaway in some cells. Turning off the cell balance also limits the discharge from the cells to minimize heating.

If this automatic response is not desired, the microcontroller can prevent an automatic shutdown of the power FETs and cell balancing operation after either an internal or external over-temperature by setting the DISITSD bit to “1” (internal temperature) or the DISXTSD bit to “1” (external temperature). In either of these cases, the IOT and XOT bits continue to indicate an over-temperature condition, but it is up to the microcontroller to detect the condition and respond.

Analog Multiplexer Selection

The ISL9216 and ISL9217 devices individually provide battery cell voltages and temperatures on the AO pin. Using the I^2C interface, the microcontroller selects the voltage to be monitored, then uses its internal A/D converter to monitor the AO voltage. See Figure 21.

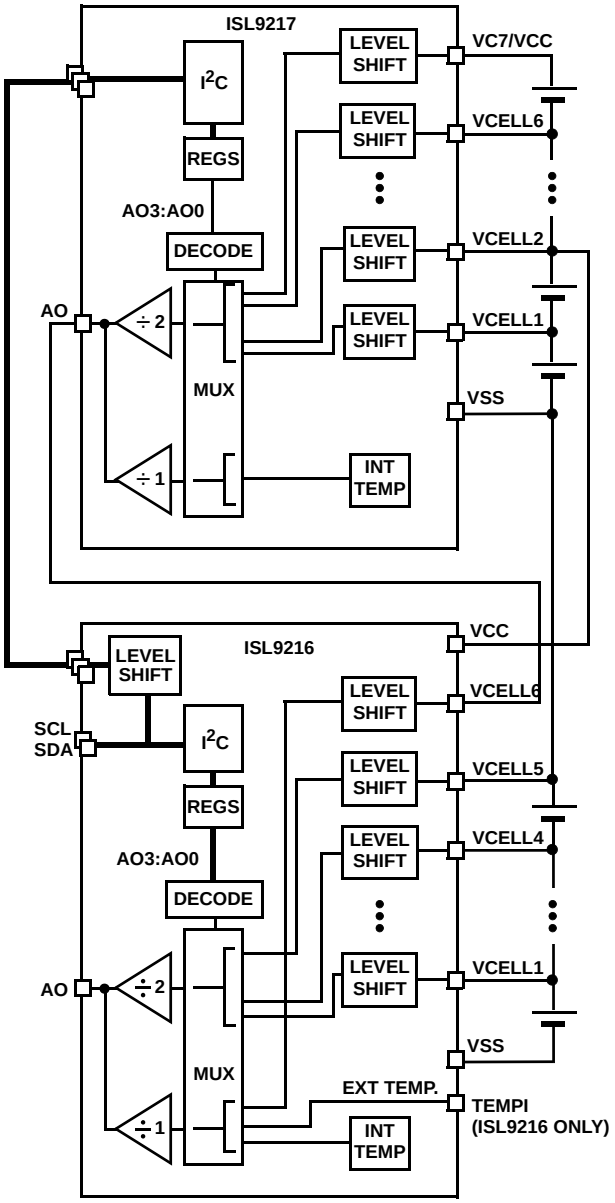


FIGURE 21. ANALOG OUTPUT MONITORING DIAGRAM

Voltage Monitoring

Since the voltage on each of the Li-ion Cells is normally higher than the regulated supply voltage, the ISL9216 and ISL9217 devices both level shifts and divide the voltage from the cells. To get into the voltage range required by the external A/D converter, the voltage level shifter divides the cell voltage by 2 (with the exception of the ISL9216 VCELL6 input). Therefore, a Li-ion cell with a voltage of 4.2V is reported via the AO pin to be 2.1V. Since the ISL9217 is not ground referenced, its AO output connects to the ISL9216 VCELL6 input and this voltage is level shifted to a ground reference.

The variation in the cell voltage from cell-to-cell is typically less than the variation from device to device. The variation of any cell voltage over the voltage range of the cells is less than the variation of the cell to cell voltage, and the variation of the output of any one cell over-temperature is even less. As such, the addition of a calibration step when testing the PCB can significantly improve the performance of the design. Following is characterization data showing the accuracy of the ISL9216 and ISL9217 individually. This data was taken over 30 units.

Figure 22 and Figure 23 show absolute error for the ISL9216 with the results of each cell compared to the input voltage. The data shows the minimum and maximum extremes of error for each cell. These figures show the device to device variation.

$$\text{Error} = (\text{Cell}_N\text{Voltage} - (\text{AO} \times 2)) - \text{Cell}_N\text{Voltage}$$

$$\text{Error} = (\text{Cell}_6\text{Voltage} - (\text{AO})) - \text{Cell}_6\text{Voltage} \quad \text{(EQ. 11)}$$

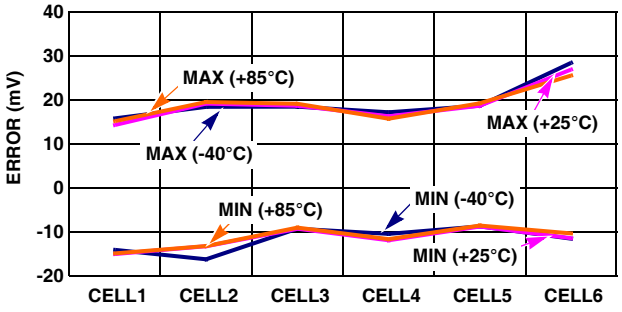


FIGURE 22. ISL9216 ANALOG OUTPUT MIN/MAX ERROR FOR 30 UNITS AT CELL VOLTAGES OF 2.3V.

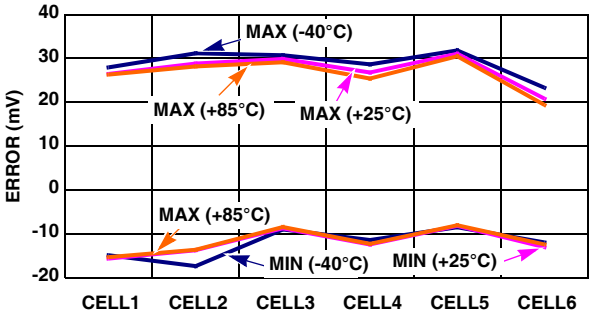


FIGURE 23. ISL9216 ANALOG OUTPUT MIN/MAX ERROR FOR 30 UNITS AT CELL VOLTAGES OF 4.3V.

Figure 24 and Figure 25 show similar results for the ISL9217.

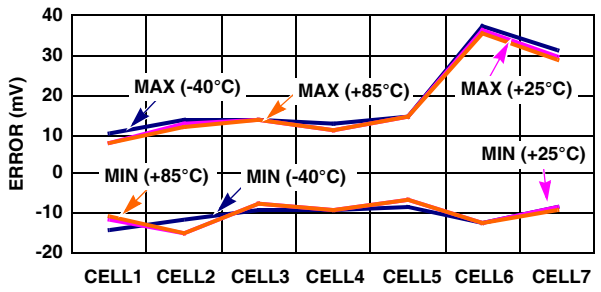


FIGURE 24. ISL9217 ANALOG OUTPUT MIN/MAX ERROR FOR 30 UNITS AT CELL VOLTAGES OF 2.3V.

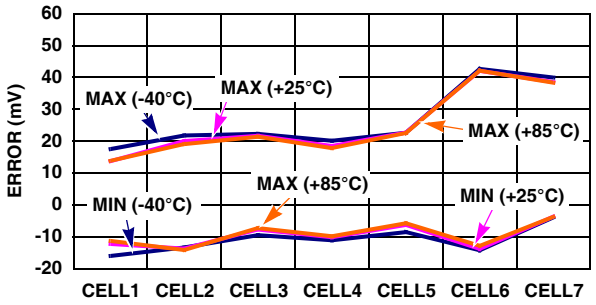


FIGURE 25. ISL9217 ANALOG OUTPUT MIN/MAX ERROR FOR 30 UNITS AT CELL VOLTAGES OF 4.3V.

For Figure 26 and Figure 27, the error for the cells on each device was compared with the error on cell3 of that same device, according to Equation 12:

$$Error = ErrorCell_N - ErrorCell_3 \quad \text{(EQ. 12)}$$

Then, the graph shows the minimum, typical, and maximum errors over the 30 units.

This gives the minimum and maximum variation of error for any one device.

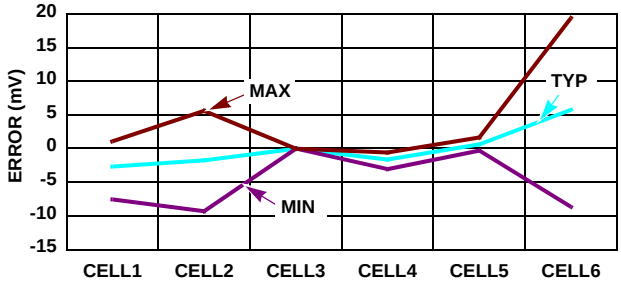


FIGURE 26. ISL9216 TYP/MIN/MAX ANALOG OUTPUT ERROR FOR 30 UNITS AT ROOM TEMPERATURE AND 2.3V CELL. ERROR RELATIVE TO CELL3.

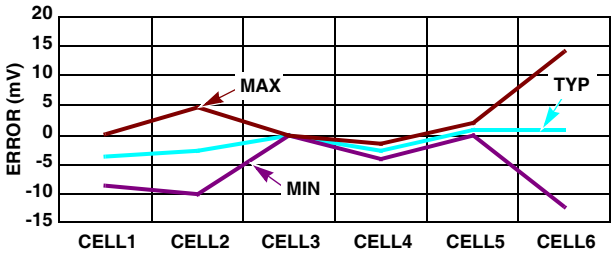


FIGURE 27. ISL9216 TYP/MIN/MAX ANALOG OUTPUT ERROR FOR 30 UNITS AT ROOM TEMPERATURE AND 4.3V CELL. ERROR RELATIVE TO CELL3.

Figure 27 and Figure 28 show similar results for the ISL9217.

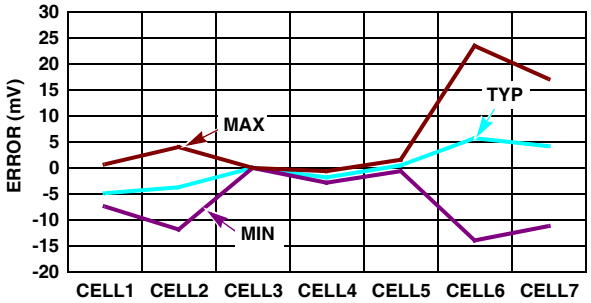


FIGURE 28. ISL9217 TYP/MIN/MAX ANALOG OUTPUT ERROR FOR 30 UNITS AT ROOM TEMPERATURE AND 2.3V CELL. ERROR RELATIVE TO CELL3.

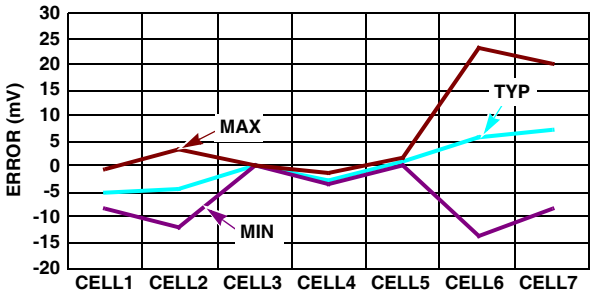


FIGURE 29. ISL9217 TYP/MIN/MAX ANALOG OUTPUT ERROR FOR 30 UNITS AT ROOM TEMPERATURE AND 4.3V CELL. ERROR RELATIVE TO CELL3.

For Figure 30, it is assumed that the error at room temperature and 4.2V per cell for each device is zero. Then the error for the cell inputs on each device at 2.3V were compared with the error on the same cell at 4.3V, according to Equation 13:

$$Error = ErrorCell_N(2.3V) - ErrorCell_N(4.2V) \quad \text{(EQ. 13)}$$

The chart then shows the minimum and maximum errors over 30 units.

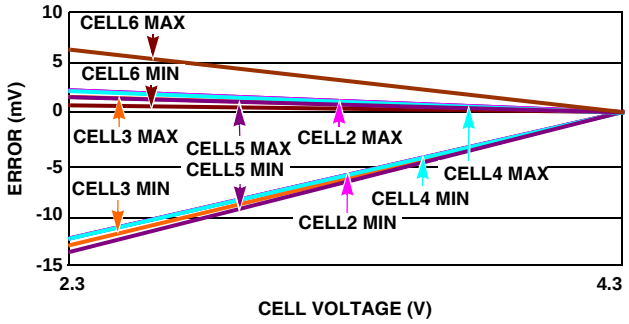


FIGURE 30. ISL9216 ANALOG OUTPUT ERROR OVER 2.3V TO 4.3V/CELL, MIN/MAX ERROR FOR 30 UNITS AT +25°C FOR CELL VOLTAGES OF 2.3V COMPARED TO 4.3V.

Figure 31 shows similar results for the ISL9217.

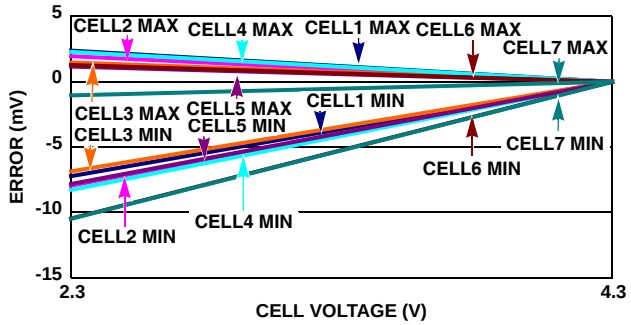


FIGURE 31. ISL9217 ANALOG OUTPUT ERROR OVER 2.3V TO 4.3V/CELL, MIN/MAX ERROR FOR 30 UNITS AT +25°C FOR CELL VOLTAGES OF 2.3V COMPARED TO 4.3V.

For Figure 32 and Figure 33, the error for the cells on each device at hot and cold were compared with the error on the same device at room temperature, according to Equation 14:

$$Error = ErrorCell_N((Hot,Cold)) - ErrorCell_N(Room) \quad \text{(EQ. 14)}$$

Then, the graph shows the minimum and maximum errors over 30 units.

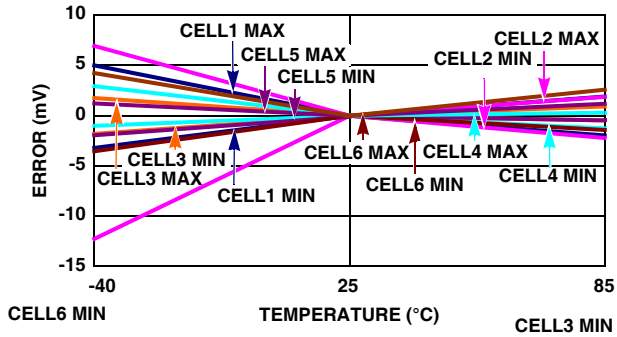


FIGURE 32. ISL9216 ANALOG OUTPUT ERROR OVER-TEMPERATURE (2.3V), MIN/MAX ERROR FOR 30 UNITS COMPARED TO ROOM TEMPERATURE FOR CELL VOLTAGES OF 2.3V.

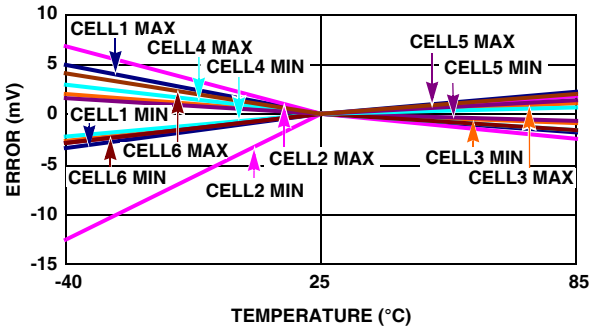


FIGURE 33. ISL9216 ANALOG OUTPUT ERROR OVER-TEMPERATURE (4.3V), MIN/MAX ERROR FOR 30 UNITS COMPARED TO ROOM TEMPERATURE FOR CELL VOLTAGES OF 4.3V.

Figure 34 and Figure 35 show similar results for the ISL9217.

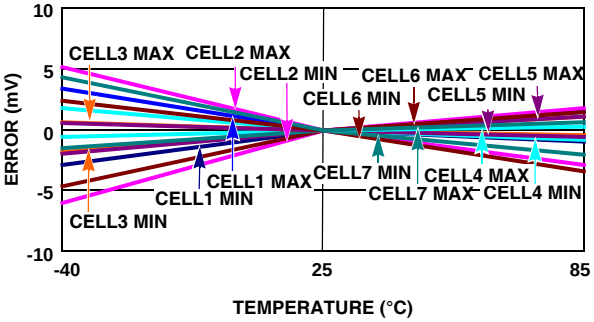


FIGURE 34. ISL9217 ANALOG OUTPUT ERROR OVER-TEMPERATURE (2.3V), MIN/MAX ERROR FOR 30 UNITS COMPARED TO ROOM TEMPERATURE FOR CELL VOLTAGES OF 2.3V.

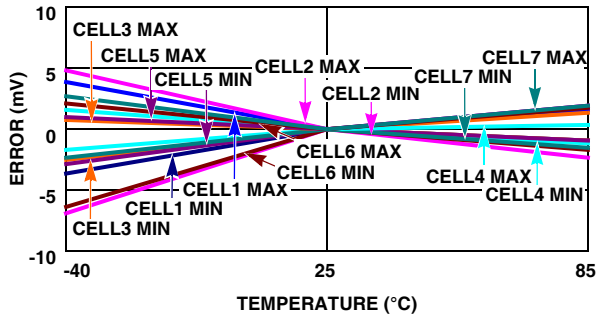


FIGURE 35. ISL9217 ANALOG OUTPUT ERROR OVER-TEMPERATURE (4.3V), MIN/MAX ERROR FOR 30 UNITS COMPARED TO ROOM TEMPERATURE FOR CELL VOLTAGES OF 4.3V.

Because the accuracy of the ISL9216 and ISL9217 is better when looking at each device, rather than assuming all devices are the same (and because the variation of the voltage measurement is less over voltage and temperature), the performance can be improved by performing a calibration at room temperature when the board is assembled.

A calibration procedure might consist of the following steps:

3. Power the board and program the microcontroller with standard pack code, using the microcontroller internal Flash and a download interface. Next, power-down the board, so on re-start the pack code is operational.
4. Apply a known voltage of 4.20V on every cell input (room temperature is fine). This powers the board and starts the microcontroller. The downloaded microcontroller code runs normally, assuming that there are no errors in the cell voltage readings. However, the code includes a calibration mode that is activated through a debugger or a dedicated pin.
5. Use the debugger or pin to start the calibration mode. Inside the microcontroller, the code successively selects each cell input. and compares the cell voltage reading with the expected 4.20V input. Any differences are temporarily stored in separate locations in RAM. Since there is a difference between readings at 4.2V and 2.3V, it is more important to calibrate at 4.2V, since accuracy is more critical when the cells are fully charged.
6. After all cell voltages are read, the code writes the offset values to Flash and uses these calibration values in future scans of the cells.

The process of powering up the board, programming it, and calibrating the inputs should take less than 15 seconds. Most of this time is taken up by the initial download of the microcontroller code and this process can be completed before connection of the board to the battery cells.

Temperature Monitoring

The voltage representing the external temperature applied at the TEMPI terminal is directed to the AO terminal through a MUX, as selected by the AO control bits (see Figure 20 and Figure 21). The external temperature voltage is not divided by 2 as are the cell voltages. Instead it is a direct reflection of the external temperature voltage divider. The microcontroller takes this monitored voltage and typically converts it to a temperature using a table. To get resolution of less than +5°C, there typically needs to be some interpolation between table set points. See some sample code in Figure 36.

A similar hardware operation occurs when monitoring the internal temperature through the AO output, except there is no external “calibration” of the voltage associated with the internal temperature. For internal temperature monitoring, the voltage at the output is linear with respect to temperature and has a slope and offset. (See the Operating Specifications for information about the output voltage at +25°C and the output slope relative to temperature). Based on the data sheet FN6488, Equation 15 translates internal temperature in volts to internal temperature in °C:

$$IntTemp^{\circ}C = \frac{AO_{IntTemp} - 1.31}{-0.0035} + 25 \qquad \text{(EQ. 15)}$$

Cell Balancing

Overview

A typical ISL9216, ISL9217 Li-ion battery pack consists of 8 to 12 cells in series, with one or more cells in parallel. This combination gives both the voltage and power necessary for power tool, e-bikes, electric wheel chairs, portable medical equipment, and battery powered industrial applications. While the series/parallel combination of Li-ion cells is common, the configuration is not as efficient as it could be, because any capacity mismatch between series connected cells reduces the overall pack capacity. This mismatch is greater as the number of series cells and the load current increase. Cell balancing techniques increase the capacity, and the operating time, of Li-ion battery packs.

There are two kinds of mismatch in the pack, State-of-Charge (SOC) and capacity/energy (C/E)[3] mismatch, with SOC mismatch being more common. Each problem limits the pack capacity (mAh) to the capacity of the weakest cell. It is important to recognize that the cell mismatch results more from limitations in process control and inspection than from variations inherent in the Lithium Ion chemistry.

The use of cell balancing can improve the performance of series connected Li-ion Cells by addressing both State-of-Charge and Capacity/Energy issues. SOC mismatch can be remedied by balancing the cell during an initial conditioning period and subsequently only during the charge phase. C/E mismatch remedies are more difficult to implement and harder to measure and require balancing during both charge and discharge periods.

Definition of Cell Balancing

Cell balancing is defined as the application of differential currents to individual cells (or combinations of cells) in a series string. Normally, of course, cells in a series string receive identical currents. A battery pack requires additional components and circuitry to achieve cell balancing.

Battery pack cells are balanced when all the cells in the battery pack meet two conditions:

1. If all cells have the same capacity, then they are balanced when they have the same relative State of Charge (SOC). In this case, the Open Circuit Voltage (OCV) is a good measure of the SOC. If, in an out of balance pack, all cells can be differentially charged to full capacity (balanced), then they will subsequently cycle normally without any additional adjustments. This is mostly a one shot fix.

3. In SOC mismatch, the cells all have the same inherent capacity, but through charge and discharge inefficiencies, they have arrived at a condition where the state of charge are different cell to cell. In C/E mismatch, the cells begin with different inherent capacities. In this type of mismatch, an imbalance between cells develops, even if there are no charge/discharge inefficiencies. Because Li-ion manufacturing is improving, the C/E mismatch is less common.

2. If the cells have different capacities, they are also considered balanced when the SOC is the same. But, since SOC is a relative measure, the absolute amount of capacity for each cell is different. To keep the cells with different capacities at the same SOC, cell balancing must provide differential amounts of current to cells in the series string during both charge and discharge on every cycle.

In an unbalanced battery pack, during charging, one or more cells will reach the maximum charge level before the rest of the cells in the series string. During discharge the cells that are not fully charged will be depleted before the other cells in the string, causing early undervoltage shutdown of the pack. These early charge and discharge limits reduce the usable charge in the battery.

Manufactured cell capacities are usually matched within 3%. If less than optimal Li-ion cells are introduced in to a series string pack or cells have been on the shelf for a long period prior to pack assembly, a 150mV difference at full charge is possible. This could result in a 13 to18% reduction in battery pack capacity.

```
/*************************************************************************************************

This function converts voltage from the AO output to external temperature. It uses a table lookup based on the muRata
NCP03XH103J05RL thermistor */


short calculate_externaltemp(short voltage)

{

unsigned short Rtable[22]={

1963, 1768, 1577, 1393, 1219, 1061, 918, 793, 682, 585, 501, 429, 368, 316, 271, 233, 201, 174, 151, 131, 114, 100

};

 char i,j;

 short temperature;

 short temp1, temp2;


 for(i=0;i<22;i++){

    if(scan_control.ISL9208Temp[0] > Rtable[i])

      break;

 }

 temperature = (-20+i*5);


 /* use the following formula to interpolate values inside a 5degree grid

 temperature = (-20+i*5) + ((scan_control.ISL9208Temp[0]-Rtable[i]) * -5)/(Rtable[i-1]-Rtable[i]);

 */

 temp1 = scan_control.ISL9208Temp[0]-Rtable[i];

 temp1 = 5*temp1;

 temp2 = Rtable[i-1]-Rtable[i];

 for(j=0;j<5;j++){

    if(temp1<(j+1)*temp2)

      break;

 }

 temperature += (4-j);


 return temperature;

}
```

FIGURE 36. SAMPLE CODE FOR CONVERTING EXTERNAL TEMP VOLTAGE TO °C

Soft Shorts

Soft shorts are the primary cause of cell imbalance in Li-ion cells. Due to tiny imperfections in cell construction the cell can have very high resistance shorts on the order of 40,000Ω or more. The self discharge rate due to this higher resistance is on the order of 0.1mA or 3% per month. Most cells do not have this condition and can hold much of their capacity for years. Some cells which meet specifications when they leave the factory may sometimes exhibit this condition later. This is strictly an electromechanical condition. Used in a single cell pack, this cell can just be recharged and shows no capacity loss. But, in a series pack, a cell with soft sorts could lose 3% per month, while another cell loses none at all. See Example 5.

Example 5: Cell balancing benefits.

Assume a 2 cell pack.
Assume cell 1 discharges 3%/month.
Assume cell 2 does has negligible discharge.
Assume the cells start at the same 40% state of charge (SOC)
Assume the pack remains on the shelf for 3 months between charging, then it is charged, discharged and charged again before again being placed on the shelf.

Compare the pack performance with and without balancing:

Results without balancing:
At 3 months: Cell1 = 31% SOC, Cell2 = 40% SOC
After charge cycle: Cell1 = 91% SOC, Cell2 = 100% SOC
After discharge cycle: Cell1 = 0% SOC, Cell2 = 9% SOC
3 month pack capacity loss = 9%.
12 month pack capacity loss = 36%. A pack that had a 3 hour run time when new, lasts only 1.9 hours after one year.

Results with balancing:
At 3 months: Cell1 = 31% SOC, Cell2 = 40% SOC
After charge cycle: Cell1 = 100% SOC, Cell2 = 100%SOC
After discharge cycle: Cell1 = 0% SOC, Cell2 = 0% SOC
3 month pack capacity loss = 0%.
12 month pack capacity loss = 0%, with only minor, recoverable, loss if not used for a long period.

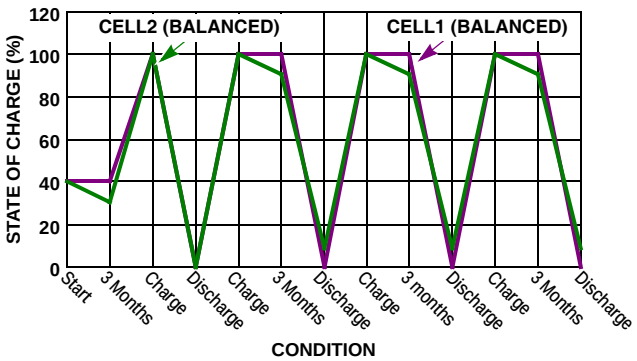


FIGURE 37. WITH CELL BALANCING

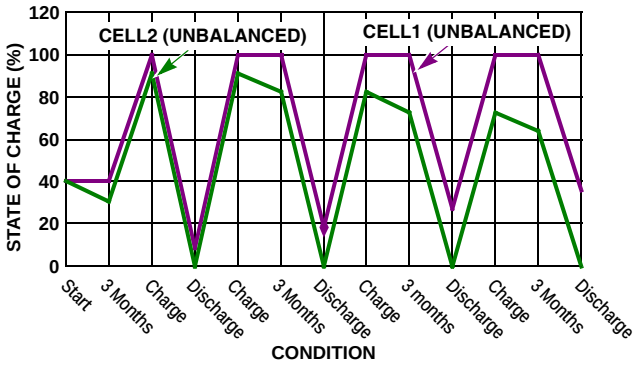


FIGURE 38. WITHOUT CELL BALANCING

Cell Balance Operation

When choosing components for the cell balancing circuit, care is needed in the selection of the external current limiting resistor to keep the currents within reasonable limits. If balancing current is too high, power dissipation can be considerable, both internally to the IC and externally in the limiting resistor. The result can be battery pack heating or component stress. If balancing current is too low, balancing takes too long or requires too many charge/discharge cycles to return a benefit. The result is ineffective or non-existent cell balancing.

The microcontroller manages cell balancing by setting a bit in the Cell Balance Register. Each bit in the register corresponds to one cell's balancing control. With the bit set, an internal cell balancing FET turns on. This shorts an external resistor across the specified cell. The maximum current that can be drawn from (or bypassed around) the cell is 200mA, based on the ISL9216, ISL9217 limits. This current is set by selecting the value of the external resistor. Figure 39 shows an example with a 200mA (maximum) balancing current.

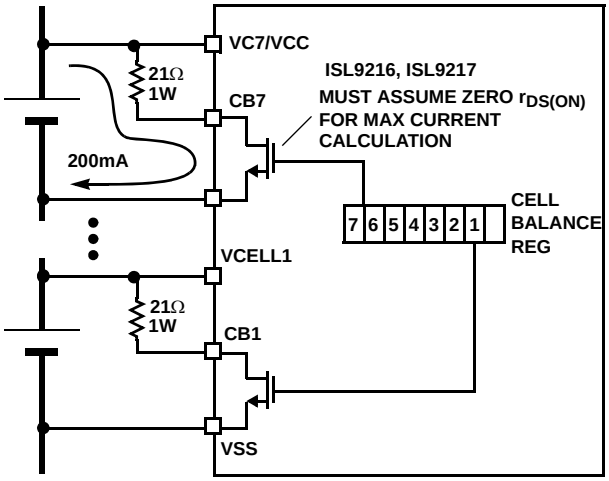


FIGURE 39. CELL BALANCING CONTROL EXAMPLE WITH 100mA BALANCING CURRENT

To program a balancing current of 200mA, start with a cell voltage of 4.2V and assume an internal resistance of 0Ω. This internal resistance is a ideal minimum $r_{DS(ON)}$. It will likely be higher, but to keep the maximum current at 200mA per cell, start with this zero internal resistance. This balancing condition calls for an external resistor of 21W. With these components, the external resistor dissipates 0.84W and the power dissipation inside the ISL9216, ISL9217 is zero. The external resistor should be sized to handle this power dissipation. (Ideally, to minimize heating, the goal is to use a 4Ω or greater resistor, but more realistically, because of board space and cost, the choice would be the use of a 2Ω resistor).

Next, to make sure the device does not dissipate too much power through the internal FET, assume an external resistor of 21Ω and an internal FET resistance of 7Ω. This gives a balancing current of 150mA (4.2V/28Ω). The external resistor in this case dissipates 0.55W and the IC FET dissipates 158mW. The ISL9216 and ISL9217 packages have a power dissipation limit of 400mW. So, because of the heat generated internally from this aggressive balancing, there should be a software limit to balance only one or two cells at a time.

With lower balancing current, more balancing FETs can be turned on at once, without exceeding the device power dissipation limits or generating excessive balancing current. A reasonable compromise between aggressive balancing and power dissipation uses a balancing current of 100mA. A 42Ω/2W cell balancing resistor sets this maximum balancing current and has a maximum power dissipation of 420mW. The internal balancing FET has a maximum dissipation of 70mW, allowing 4 to 5 cell balancing FETs to be on at the same time.

The above calculations are for maximum cell voltages. But, as the cell voltage drops, the overall power dissipation also drops.

The ISL9216, ISL9217 devices support battery packs with multiple cells in parallel. With more than 2 cells in parallel, however, cell balancing becomes more difficult due to the higher pack capacities. At these higher capacities, the maximum 200mA balancing current limits the rate of balancing. To deal with this, an external P-Channel FET can be used to provide higher currents. Figure 40 shows an example of such a circuit. In this case it is even more important to separate the voltage monitoring and cell balancing paths to get accurate readings of the cell voltage while cell balancing is on. This connection of cell balancing components completely isolates the cell balancing from the cell monitoring, so in this case monitoring and balancing can be performed simultaneously.

Another design consideration is to choose an external P-Channel FET with a gate turn on voltage below the minimum cell voltage that balancing will take place. For example, if the cells will be balanced down to 2.5V, then the FET turn on voltage needs to be less than 2.5V. The circuit of Figure 40 provides up to 400mA of balancing current. This requires the use of 5W balancing resistors and 1W cell balancing transistors.

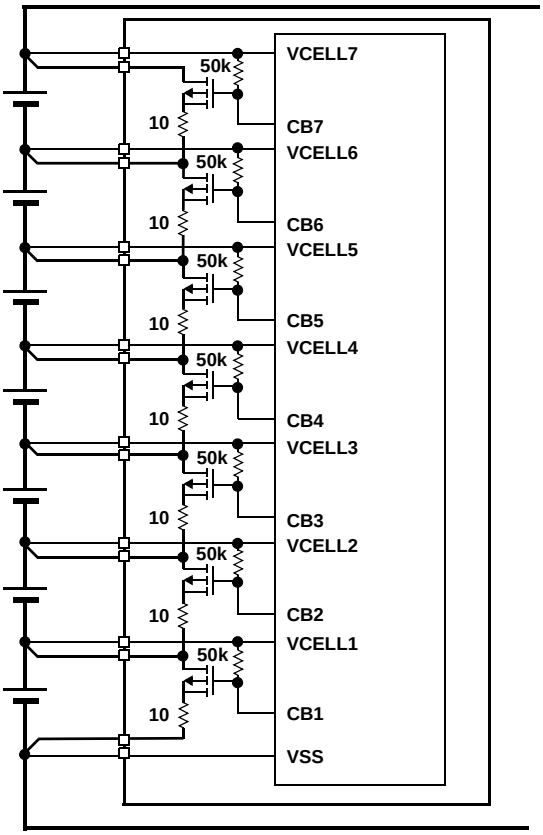


FIGURE 40. HIGH CURRENT CELL BALANCING CIRCUIT

Cell Balance Control Algorithm

Designing the software for cell balancing can become quite difficult as there are several limitations that should be considered and several difficult obstacles to overcome. Some of the design elements of cell balancing are listed in the following:

1. **Maximum voltage differential between cells.** If the difference between the cells is too great, it could indicate that there is a bad cell. In this case, the decision by the microcontroller code might be to shut down the pack.
2. **Minimum voltage differential between cells.** If the cell voltage differential is too small, then it could be said the cells are already balanced. The decision about what voltage differential is too small is primarily based on the accuracy of the voltage measurement system. If the error in the measurement system is greater than the minimum cell balance differential, then a cell could be balanced that did not need to be, and the cell imbalance can increase.
3. **Temperature limits on balancing.** It is usually desirable to refrain from balancing when the cells are too hot or too cold. When cells are too hot, balancing them could increase the temperature of the cells. When cells are too cold charging should be restricted, limiting the opportunities for balancing.

4. **Maximum and minimum voltage on the individual cells being balanced.** This is not usually a problem and cells can be balanced all the way from the under charge level to the over charge level. However, if the balancing operation affects the cell measurement, then operating the cell balancing algorithm at the capacity extremes may cause significant changes in the observed cell voltage, leading to pack shut down or resulting in the attempted balance of cells that do not need balancing. Also, as the cell voltages near their maximum, it is necessary to keep a close watch on the voltage, to avoid over charging the cells. It may not be possible to balance at the same time as closely monitor the cells near the over charge limit.
5. **Balancing on-time vs off-time.** Ideally, there would not need to be a balancing on and off time. However, without using external balancing FETs, any significant balancing current will affect the voltage at the ISL9216, ISL9217 VCELLN pins when the balancing is turned on. Adding a separate “Kelvin” connection from the terminal of the cell to the VCELLN pin (see Figure 1 and Figure 40), minimizing resistance in the cell to board connections, and balancing with less current all reduce the measurement error. But, in general, the cell balance circuit must turn off periodically for the microcontroller to get a good reading of the cell voltages for managing the over charge and under charge condition of the cells as well as to determine the continuing need for cell balancing.
6. **Maximum number of cells balanced at a time.** As mentioned earlier, the total number of cells balanced at any one time may be limited by the package power dissipation levels. This needs to be comprehended in the algorithm.
7. **Balancing order.** The algorithm normally sorts the cell voltages in order from high to low. Then, if the difference between any higher voltage cell and the minimum voltage cell exceeds the minimum balancing differential, then that cell balance is turned on. The algorithm starts by turning on the highest voltage cell, then the next highest, and so on until the maximum number of balanced cells is reached or no additional cells have a high enough voltage differential.
8. **Balance during charge or discharge or both.** Balancing cells during discharge conditions is not common. In this case charge from the pack is “burned” in the balancing resistors during a period where maximum energy is required. Balancing during discharge reduces the pack capacity in the short term. It could be that this short term loss results in a long term gain, if the cells can be balanced quickly, but it is not obvious that this is the case.

   Balancing cells during the charge condition is the more common technique, since there is energy available from the charger to replenish that lost through the cell balance resistors. By balancing during charge, it is necessary to increase the charge current slightly to keep the overall charge time from increasing.

   The best method of implementing cell balancing during charge is to include a communication path between the pack microcontroller and the charger. This communication path allows the charger to monitor individual cell voltages, but it also allows the charger to let the pack know that a charger is present so balancing can commence.

   Without a charger communication path, in a two terminal pack for example, the microcontroller code inside the pack needs to detect the presence of a charging current or use the pack voltage and cell voltages to determine if a charger is connected or not. This is not a trivial solution.

   A modification of the FET desaturation current circuit in Figure 17 on page 12 could be used to provide the microcontroller an indication of charge current. In this case, the microcontroller would monitor the voltage at point A. When this voltage drops significantly from the voltage when there is no current, then the microcontroller concludes that a charge is in progress.

   Without this hardware indication, the pack can use an instantaneous change in the pack voltage to detect that a charger is connected. This instantaneous change can be several hundred millivolts when the charger connects. However, this change in pack voltage can be indistinguishable from the change in pack voltage caused by the instantaneous drop in the load current.

   The pack can use an average dV/dt of the pack voltage to determine if the pack is charging or discharging. A pack being discharged generates a negative dV/dt; a pack being charged creates a positive value. However, in this case the pack voltage needs to be filtered to avoid noise in the measurements and to smooth out short term variations in the load. The dV/dt value also needs to be averaged over a period of time, because in the middle of the cell voltage range there can be a lot of capacity change with very little corresponding voltage change. In this case, cell balancing could automatically stop if the dV/dt detection returns a zero charge rate.

Pack Communications

If it is important to communicate with the pack microcontroller from the outside world, the easiest method is with a two wire interface such as the SMBus or I2C bus. Most microcontrollers have one of these interfaces implemented in hardware. Alternatively, a one-wire interface could be developed, using microcontroller code.

Another design consideration for communication is that the microcontroller is ground referenced at the same point as the ISL9216. When the power FETs are off, this ground reference is different from the PACK- point. So, communication between the pack and outside are only possible in the following conditions:

1. The power FETs are on. In this case, the PACK- terminal is roughly the same potential as the microcontroller ground.

2. The 2-wire external communication connector also provides the microcontroller ground voltage, so it is not necessary that the power FETs be on. CAUTION: In this case, the unit communicating with the pack cannot also use the PACK- terminal as a ground connection. The PACK- terminal should be floating. Otherwise, when the power FETs turn off, either an unsafe voltage differential occurs between the microcontroller ground and the PACK- pin, potentially damaging the microcontroller, or the monitoring device provides a discharge path around the power FETs. Neither condition is desired.

   Keep in mind also that a PC (for monitoring) and a power supply (for charging) may have their grounds connected together through their chassis and the AC power connection. The same is true if a scope is connected to the board. This may not be obvious. So using both of these units in the second configuration may require extra attention.

If monitoring of the pack is desired in production, then option 2 is normally sufficient. If a charger needs to communicate with the pack, then option 1 is required and the pack microcontroller needs to turn on the power FETs before communication is possible. If the pack shuts down because of an over charge condition, the over charge condition must be resolved before communication is re-established.

Other Design Ideas

The following design ideas are proposed implementations and have not been thoroughly tested and will likely require additional software control.

Input Filtering

In some applications it is required that the cell inputs be filtered before being monitored by the ISL9216, ISL9217. As mentioned earlier, this will add an offset error to the monitored input voltage. However, if the microcontroller can perform a calibration on initial assembly and can store this value in non-volatile memory, then it is possible to add filters to the inputs.

Adding a series resistance to each input, as part of the input filter, has one other negative. It adds resistance to the cell balance path. This both reduces the available cell balance current and creates an even larger measurement error when the cells are being balanced. As such, this design option requires the addition of external P-Channel FETs for balancing. These extra FETs add some cost to the system, but will allow higher balancing current.

The combined input filter and external cell balancing input are shown in Figure 41. In this case, the 1kΩ resistors add about 120mV error to the readings for cell2 through cell6 (depending on the input), about 60mV error on cell1 input, and about 6mV error on cell7.

This error on the inputs is due to a current that flows when sampling the cell voltage. The current varies cell to cell, but it is consistent for any specific cell input.

The cell7 input poses a more difficult problem, because the error varies according to the current consumption of the ISL9216 and ISL9217 device. However, if the series resistor is kept small, then there will likely be very little variation in the current consumption (for any specific device) at the time when a measurement is being made.

There is one additional advantage to this input connection. That is, the ISL9216, ISL9217 is protected against input surge currents, so it is possible to connect the cells to the PCB in any sequence.

Positive Edge Wakeup Variations

When used in a power tool application, the positive edge wake up might be used to power down the pack when it is removed from the tool or the charger.

Positive edge wake up might also be used such that the WKUP pin is connected directly to the power tool switch so the pack is always asleep until the switch is pulled. In this case, care should be taken with the microcontroller software so the code wakes up quickly enough that there is no perceived lag on the trigger pull. This connection will also cause the FETs to turn on during a condition of maximum current.

In some other applications, the WKUP pin could be connected to a system control signal. In this case, the pack is powered down when not needed, for example when the unit is taken off-line. Then, when the unit is again placed in service, a signal can be sent to the battery pack to wake it up. This provides maximum life of the battery when the system does not require battery operation.

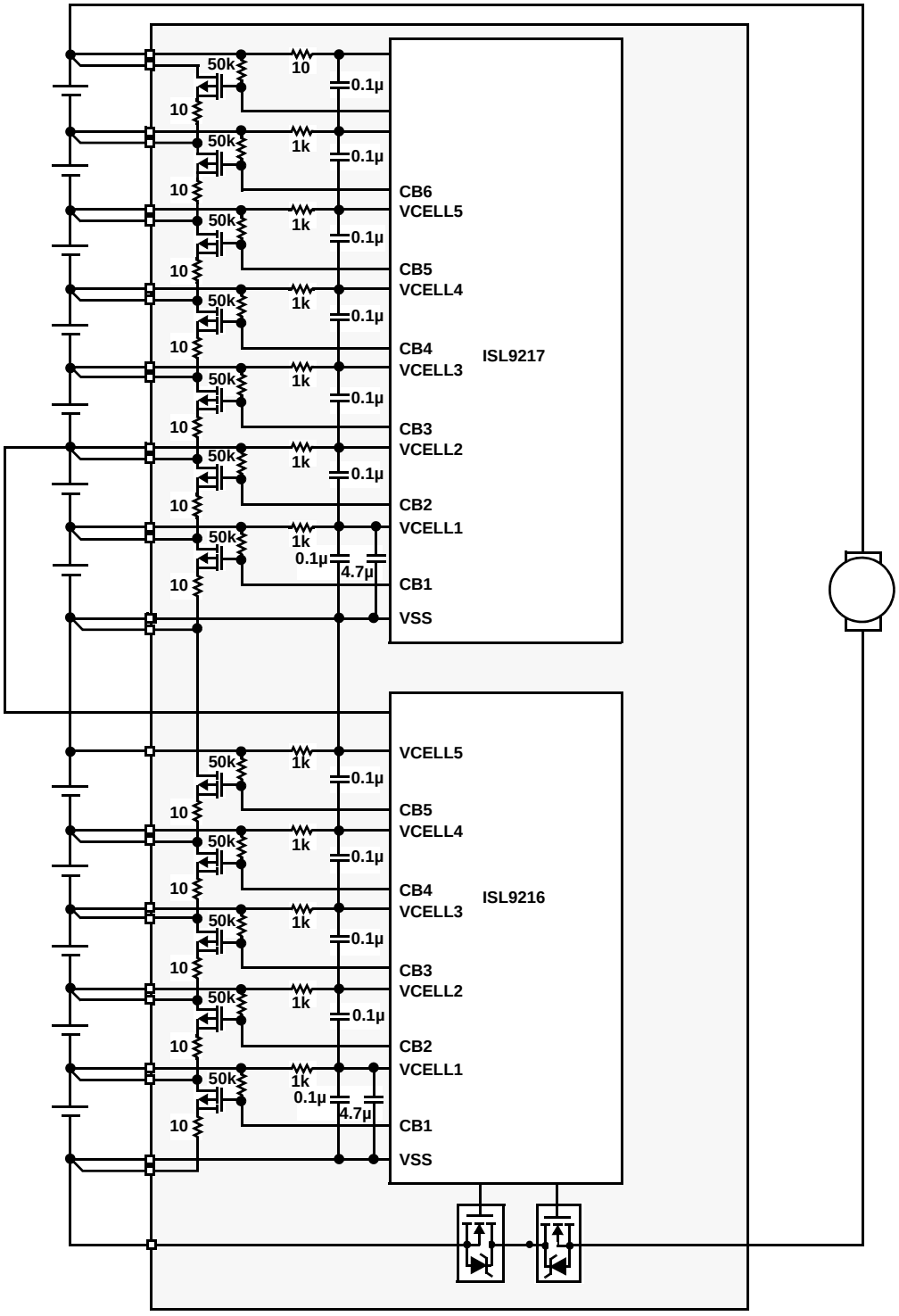


FIGURE 41. SIMPLIFIED DIAGRAM OF INPUT FILTER/EXTERNAL BALANCING FETS

Packs with more than 12 Series Connected Cells

For applications that require more than 12-series connected cells, the ISL9216, ISL9217 chip set needs to be connected with additional level shifters or isolation circuits to allow cascading multiple battery modules in a single pack. For example, a pack with 24 series connected cells could use two ISL9216, ISL9217 modules (See Figure 42). This example shows optical isolation, which will work with many modules, but for 2 modules only, this pack can be also be done with FET level shifters.

The ISL9216, ISL9217 cannot support a pack with 14-series connected cells in its normal configuration. However, there are two possible approaches to this pack. In the first, two ISL9208 devices are cascaded (See Figure 43). Each of these support 7 cells and each has a microcontroller managing the module operation. The microcontroller for the lower ISL9208 also includes communication with the upper module through level shifting circuitry. In this case, the level shifter is implemented with several FETs. This technique could be used with multiple cascaded ISL9208s, but there is a limit due to voltage ratings of the FETs. The level shifter could be replaced with an optical isolator for virtually unlimited cascading.

In a second method of implementing a 14-cell series connected pack, an ISL9208 is used with an ISL9217 and only one microcontroller (See Figure 44). The ISL9217 was selected in this case, because it has a “split” I2C interface with an SDA_{OUT} and an SDA_{IN}. This is easier to handle when level shifting than a bidirectional port. The ISL9217 also does not include the FET control functions which are not needed on the upper cascaded devices. The ISL9208 was selected over the ISL9216, because the ISL9216 only monitors up to 5-cells.

This circuit also shows a mechanism for level shifting the analog output of the ISL9217 to a ground reference so it can be monitored by the ISL9208 microcontroller. The AO level shifter has three main sources for error. The op amp offset error translates to an offset error at the microcontroller analog input. A current mirror mismatch and a mismatch between resistors R_1 and R_2 each translates to a gain error at the microcontroller.

These 14-cell design ideas have not been implemented and are presented here for purposes of discussion only.

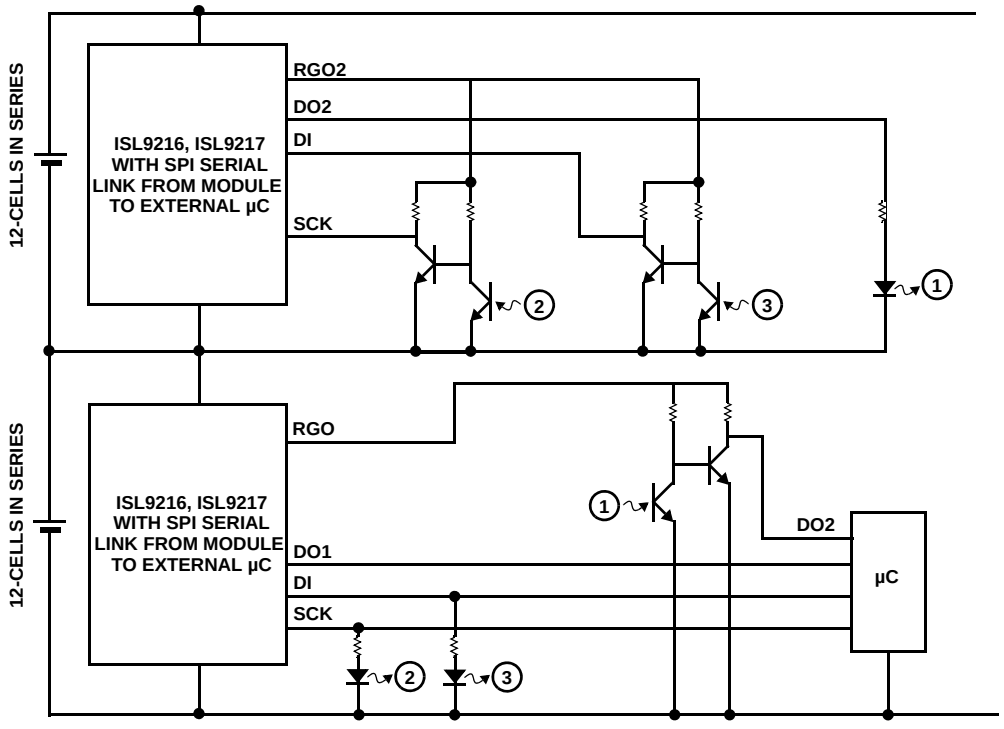


FIGURE 42. 24-CELL SERIES BATTERY PACK USING TWO ISL9216, ISL9217 MODULES AND OPTICAL ISOLATION

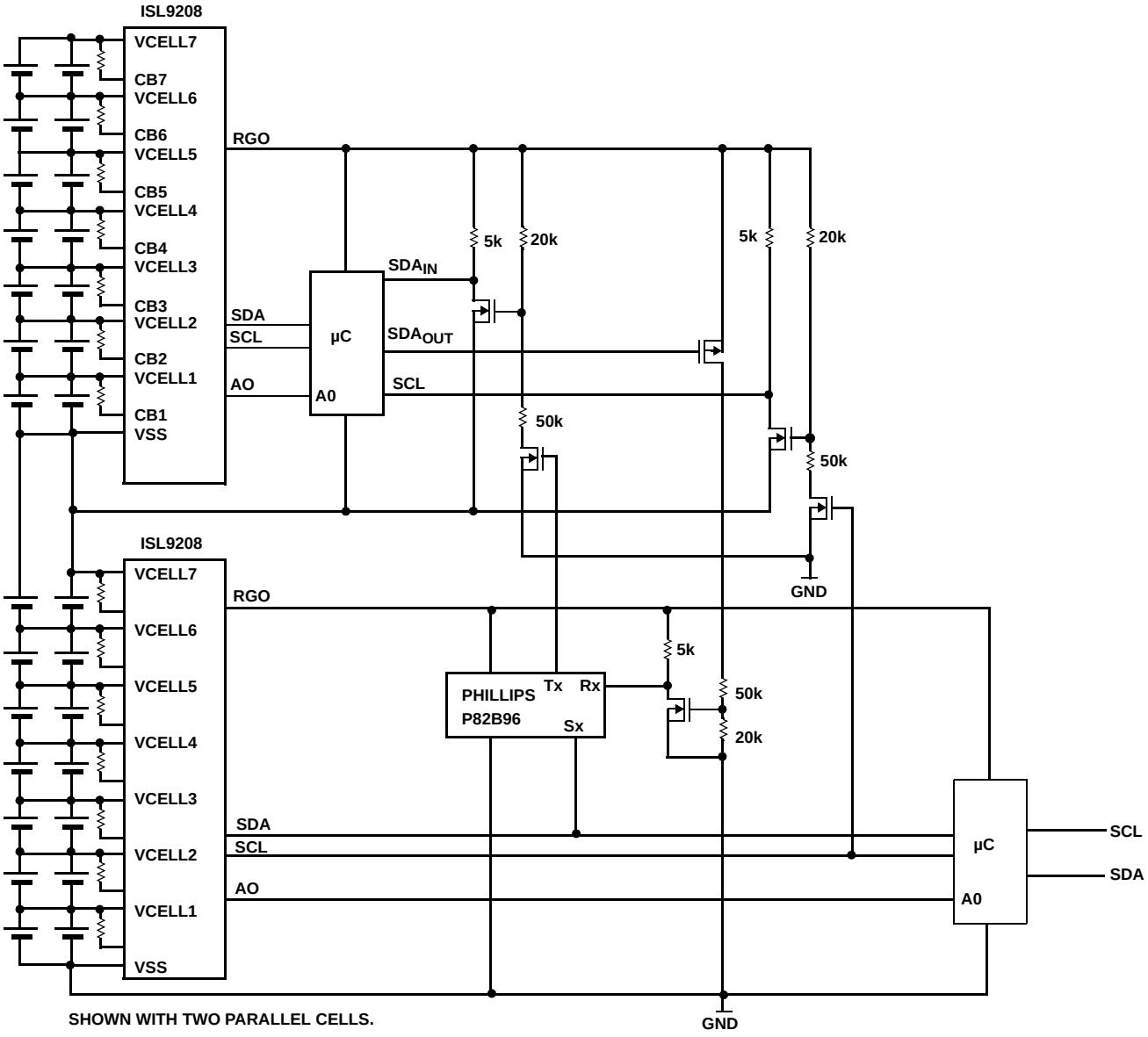
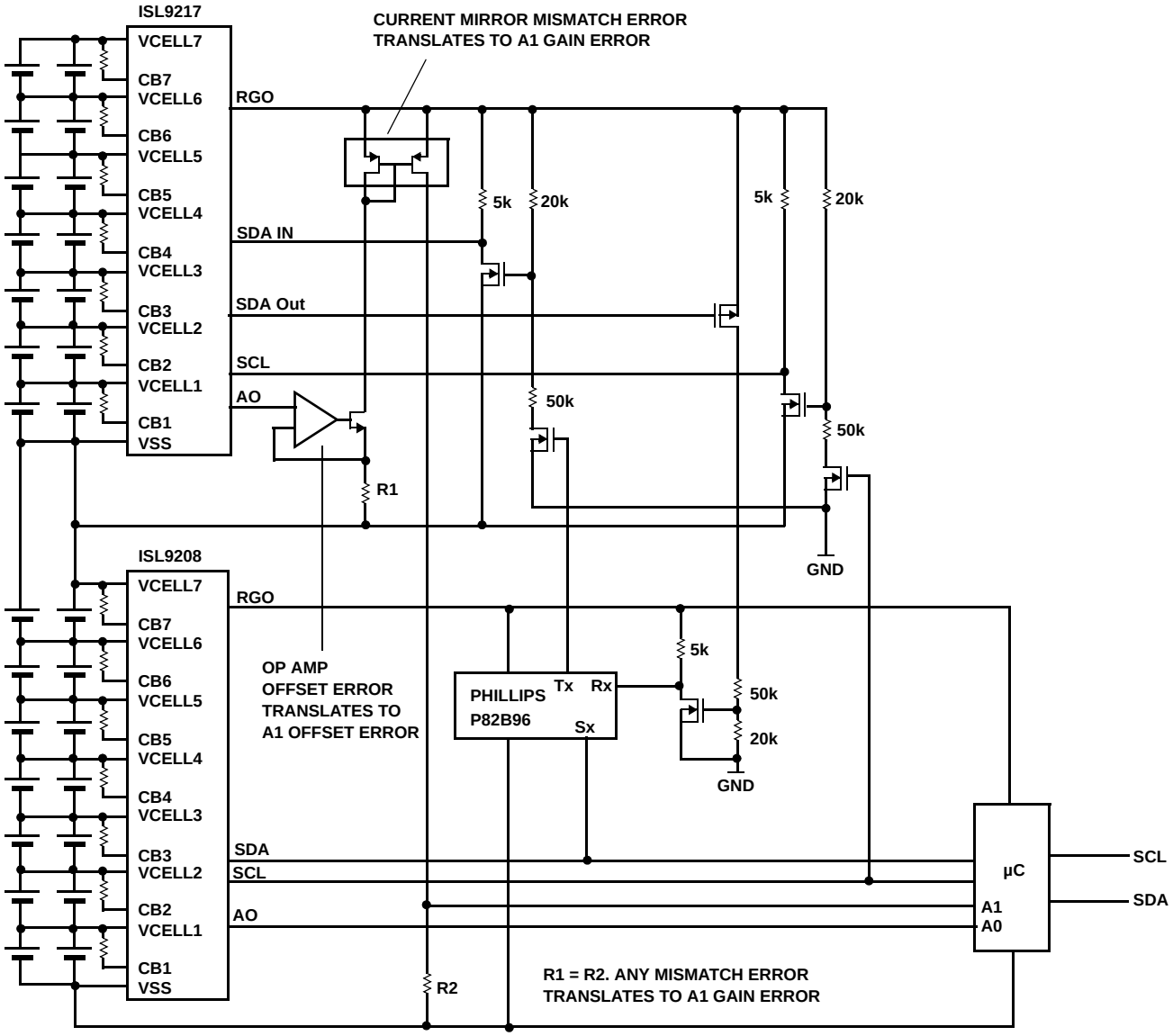


FIGURE 43. USING TWO ISL9208 DEVICES TO IMPLEMENT A 14-CELL SERIES CONNECTED PACK



Shown with two parallel cells.

FIGURE 44. USING AN ISL9208 AND ISL9217 TO IMPLEMENT A 14-CELL SERIES CONNECTED PACK

Battery Pack Software

There are many things to consider when writing the software for a battery pack controller. Please see the ISL9216EVAL1 Software user guide for more detailed information about battery pack code implementation.